

Compal Confidential

ICL50/51, ICK70/71 Schematics Document

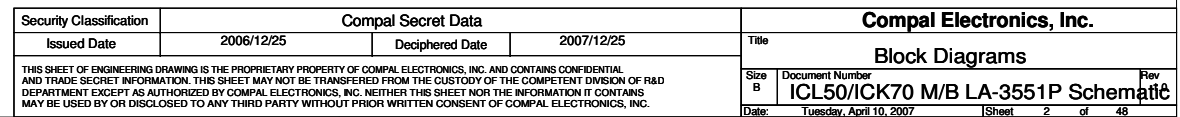
Intel Merom Processor with Crestline(PM965/GM965) + DDRII + ICH8M
(With ATI MXM/B)

2007-4-4

REV: 1.0

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				Date: Tuesday, April 10, 2007	Rev Sheet 1 of 48

Model Name : ICL50/51, ICK70/ICK71
File Name : LA-3551P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394/Card Reader	AD16	0	PIRQE PIRQG

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

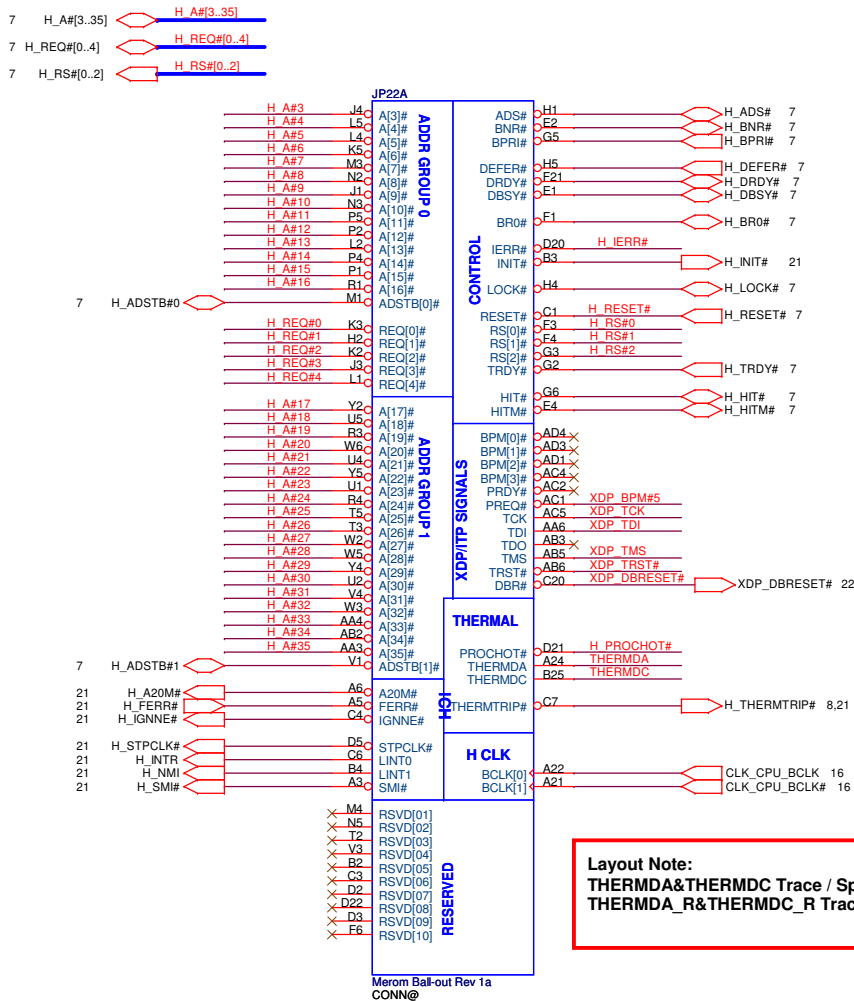
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

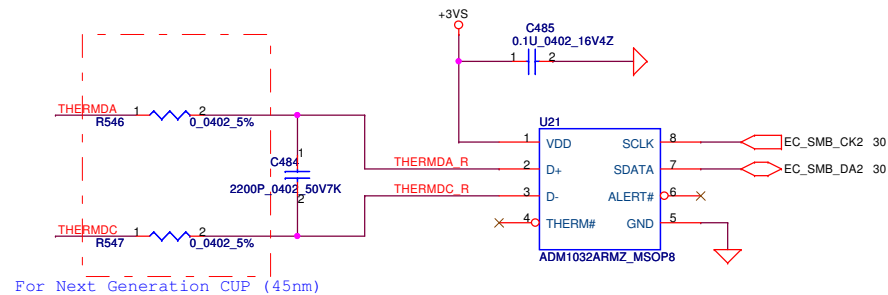
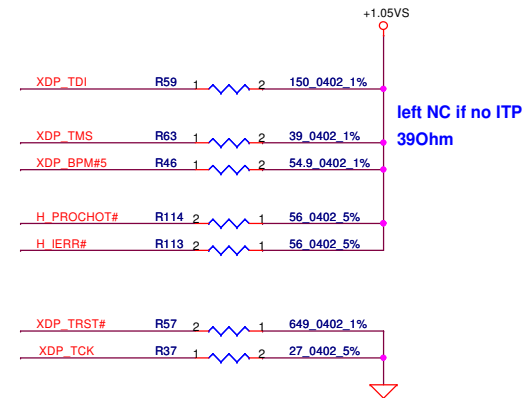
BTO Option Table

BTO Item	BOM Structure
Discrete	PM@
UMA	GM@



BSEL2	BSEL1	BSEL0	BCLK
0	1	0	200
0	1	1	166

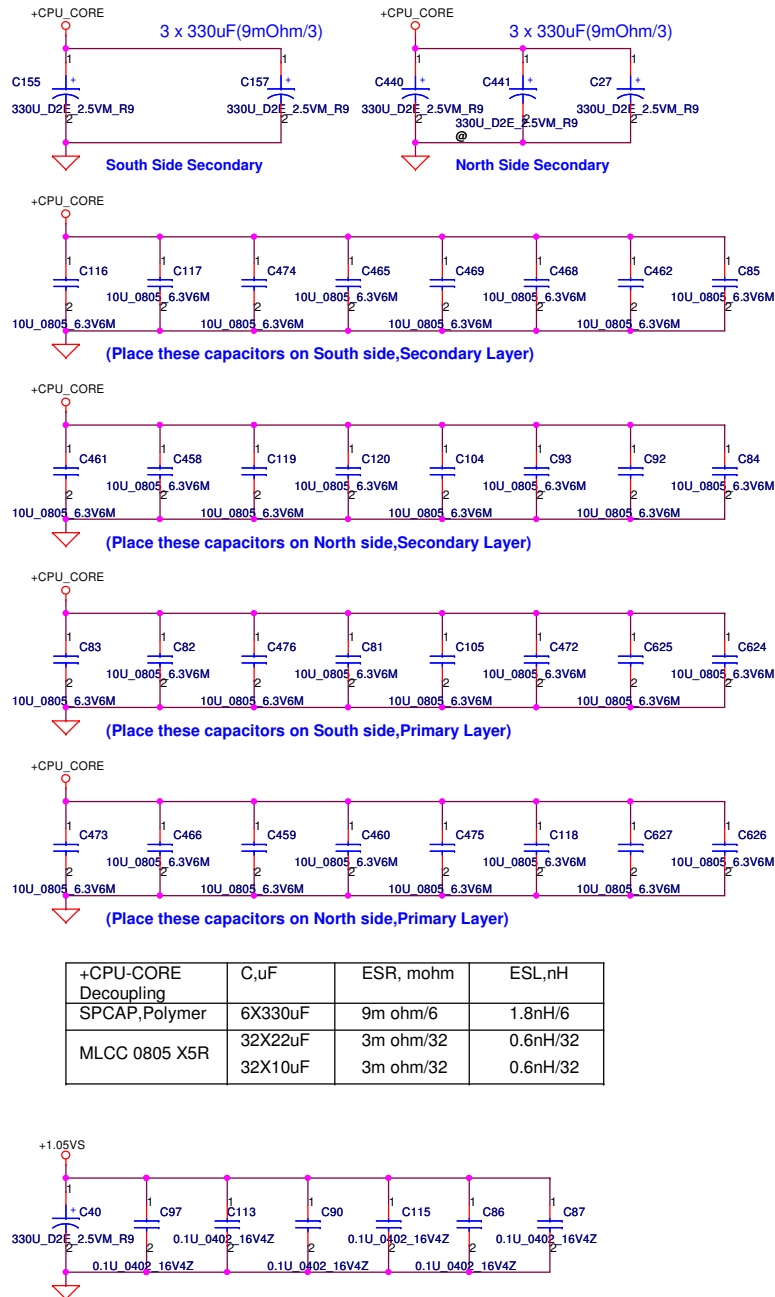
Layout Note:
THERMDA&THERMDC Trace / Space = 10 / 10 mil
THERMDA_R&THERMDC_R Trace / Space = 10 / 10 mil



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								Merom (1/3)	
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JP22D			
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	A25
		VSS[163]	AF25

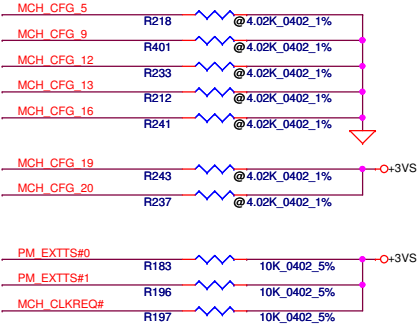
Merom Ball-out Rev 1a
CONN@



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CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present



14 DDRA_SDQ[0..63] <== DDRA_SDQ[0..63]
14 DDRA_SDM[0..7] <== DDRA_SDM[0..7]
14 DDRA_SMA[0..13] <== DDRA_SMA[0..13]

15 DDRB_SDQ[0..63] <== DDRB_SDQ[0..63]
15 DDRB_SDM[0..7] <== DDRB_SDM[0..7]
15 DDRB_SMA[0..13] <== DDRB_SMA[0..13]

U23D
DDRA_SDQ0 AR43 SA_DQ_0
DDRA_SDQ1 AW44 SA_DQ_1
DDRA_SDQ2 BA45 SA_DQ_2
DDRA_SDQ3 AY46 SA_DQ_3
DDRA_SDQ4 AB41 SA_DQ_4
DDRA_SDQ5 AR45 SA_DQ_5
DDRA_SDQ6 AT42 SA_DQ_6
DDRA_SDQ7 AW47 SA_DQ_7
DDRA_SDQ8 BB45 SA_DQ_8
DDRA_SDQ9 BF48 SA_DQ_9
DDRA_SDQ10 BG47 SA_DQ_10
DDRA_SDQ11 BA45 SA_DQ_11
DDRA_SDQ12 BB47 SA_DQ_12
DDRA_SDQ13 BG50 SA_DQ_13
DDRA_SDQ14 BH49 SA_DQ_14
DDRA_SDQ15 BE45 SA_DQ_15
DDRA_SDQ16 AW43 SA_DQ_16
DDRA_SDQ17 BE42 SA_DQ_17
DDRA_SDQ18 BC42 SA_DQ_18
DDRA_SDQ19 BE40 SA_DQ_19
DDRA_SDQ20 BF44 SA_DQ_20
DDRA_SDQ21 BH45 SA_DQ_21
DDRA_SDQ22 BG40 SA_DQ_22
DDRA_SDQ23 BF40 SA_DQ_23
DDRA_SDQ24 AB40 SA_DQ_24
DDRA_SDQ25 AW40 SA_DQ_25
DDRA_SDQ26 AT39 SA_DQ_26
DDRA_SDQ27 AW36 SA_DQ_27
DDRA_SDQ28 AW41 SA_DQ_28
DDRA_SDQ29 AY41 SA_DQ_29
DDRA_SDQ30 AY38 SA_DQ_30
DDRA_SDQ31 AT38 SA_DQ_31
DDRA_SDQ32 AV13 SA_DQ_32
DDRA_SDQ33 AT13 SA_DQ_33
DDRA_SDQ34 AW11 SA_DQ_34
DDRA_SDQ35 AV11 SA_DQ_35
DDRA_SDQ36 AU15 SA_DQ_36
DDRA_SDQ37 AT11 SA_DQ_37
DDRA_SDQ38 BA13 SA_DQ_38
DDRA_SDQ39 BA11 SA_DQ_39
DDRA_SDQ40 BE10 SA_DQ_40
DDRA_SDQ41 BD10 SA_DQ_41
DDRA_SDQ42 BD8 SA_DQ_42
DDRA_SDQ43 AY9 SA_DQ_43
DDRA_SDQ44 BG10 SA_DQ_44
DDRA_SDQ45 AW9 SA_DQ_45
DDRA_SDQ46 BD7 SA_DQ_46
DDRA_SDQ47 BB9 SA_DQ_47
DDRA_SDQ48 BB5 SA_DQ_48
DDRA_SDQ49 AT5 SA_DQ_49
DDRA_SDQ50 AT5 SA_DQ_50
DDRA_SDQ51 AY6 SA_DQ_51
DDRA_SDQ52 BB7 SA_DQ_52
DDRA_SDQ53 AR5 SA_DQ_53
DDRA_SDQ54 AR5 SA_DQ_54
DDRA_SDQ55 AR8 SA_DQ_55
DDRA_SDQ56 AR8 SA_DQ_56
DDRA_SDQ57 AN3 SA_DQ_57
DDRA_SDQ58 AM8 SA_DQ_58
DDRA_SDQ59 AN10 SA_DQ_59
DDRA_SDQ60 AT9 SA_DQ_60
DDRA_SDQ61 AN9 SA_DQ_61
DDRA_SDQ62 AM9 SA_DQ_62
DDRA_SDQ63 AN11 SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0 BB19 <== DDRA_SBS0# 14
SA_BS_1 BK19 <== DDRA_SBS1# 14
SA_BS_2 BE29 <== DDRA_SBS2# 14
SA_CAS# BL17 <== DDRA_SCAS# 14
SA_DM_0 AT45 <== DDRA_SDM0
SA_DM_1 BD44 <== DDRA_SDM1
SA_DM_2 BD42 <== DDRA_SDM2
SA_DM_3 AW38 <== DDRA_SDM3
SA_DM_4 AW13 <== DDRA_SDM4
SA_DM_5 BG8 <== DDRA_SDM5
SA_DM_6 AY5 <== DDRA_SDM6
SA_DM_7 AN6 <== DDRA_SDM7
SA_DQS_0 AT46 <== DDRA_SDQS0
SA_DQS_1 BE48 <== DDRA_SDQS1
SA_DQS_2 BB43 <== DDRA_SDQS2
SA_DQS_3 BC37 <== DDRA_SDQS3
SA_DQS_4 BB16 <== DDRA_SDQS4
SA_DQS_5 BH6 <== DDRA_SDQS5
SA_DQS_6 BB2 <== DDRA_SDQS6
SA_DQS_7 AP3 <== DDRA_SDQS7
SA_DQS#_0 AT47 <== DDRA_SDQS0#
SA_DQS#_1 BD47 <== DDRA_SDQS1#
SA_DQS#_2 BC41 <== DDRA_SDQS2#
SA_DQS#_3 BA37 <== DDRA_SDQS3#
SA_DQS#_4 BA16 <== DDRA_SDQS4#
SA_DQS#_5 BH7 <== DDRA_SDQS5#
SA_DQS#_6 BC1 <== DDRA_SDQS6#
SA_DQS#_7 AP2 <== DDRA_SDQS7#
SA_MA_0 BJ19 <== DDRA_SMA0
SA_MA_1 BD20 <== DDRA_SMA1
SA_MA_2 BK27 <== DDRA_SMA2
SA_MA_3 BH28 <== DDRA_SMA3
SA_MA_4 BL24 <== DDRA_SMA4
SA_MA_5 BK28 <== DDRA_SMA5
SA_MA_6 BJ27 <== DDRA_SMA6
SA_MA_7 BJ25 <== DDRA_SMA7
SA_MA_8 BL28 <== DDRA_SMA8
SA_MA_9 BA28 <== DDRA_SMA9
SA_MA_10 BC19 <== DDRA_SMA10
SA_MA_11 BE28 <== DDRA_SMA11
SA_MA_12 BG30 <== DDRA_SMA12
SA_MA_13 BJ16 <== DDRA_SMA13
SA_RAS# BE18 <== DDRA_SRAS# 14
SA_RCVEN# AY20 <== DDRA_SRCVEN# PAD T13
SA_WE# BA19 <== DDRA_SWE# 14

CRESTLINE_1p0

PM@

U23E
DDRBD_SDQ0 AP49 SB_DQ_0
DDRBD_SDQ1 AR51 SB_DQ_1
DDRBD_SDQ2 AW50 SB_DQ_2
DDRBD_SDQ3 AW51 SB_DQ_3
DDRBD_SDQ4 AN51 SB_DQ_4
DDRBD_SDQ5 AN50 SB_DQ_5
DDRBD_SDQ6 AV50 SB_DQ_6
DDRBD_SDQ7 AV49 SB_DQ_7
DDRBD_SDQ8 BA50 SB_DQ_8
DDRBD_SDQ9 BB50 SB_DQ_9
DDRBD_SDQ10 BA49 SB_DQ_10
DDRBD_SDQ11 BE50 SB_DQ_11
DDRBD_SDQ12 BA51 SB_DQ_12
DDRBD_SDQ13 AY49 SB_DQ_13
DDRBD_SDQ14 BE50 SB_DQ_14
DDRBD_SDQ15 BF49 SB_DQ_15
DDRBD_SDQ16 BJ50 SB_DQ_16
DDRBD_SDQ17 BJ44 SB_DQ_17
DDRBD_SDQ18 BJ43 SB_DQ_18
DDRBD_SDQ19 BL43 SB_DQ_19
DDRBD_SDQ20 BK47 SB_DQ_20
DDRBD_SDQ21 BK49 SB_DQ_21
DDRBD_SDQ22 BK43 SB_DQ_22
DDRBD_SDQ23 BK42 SB_DQ_23
DDRBD_SDQ24 BJ41 SB_DQ_24
DDRBD_SDQ25 BL41 SB_DQ_25
DDRBD_SDQ26 BJ37 SB_DQ_26
DDRBD_SDQ27 BJ36 SB_DQ_27
DDRBD_SDQ28 BK41 SB_DQ_28
DDRBD_SDQ29 BJ40 SB_DQ_29
DDRBD_SDQ30 BL35 SB_DQ_30
DDRBD_SDQ31 BK37 SB_DQ_31
DDRBD_SDQ32 BK13 SB_DQ_32
DDRBD_SDQ33 BE11 SB_DQ_33
DDRBD_SDQ34 BK11 SB_DQ_34
DDRBD_SDQ35 BC11 SB_DQ_35
DDRBD_SDQ36 BC13 SB_DQ_36
DDRBD_SDQ37 BE12 SB_DQ_37
DDRBD_SDQ38 BC12 SB_DQ_38
DDRBD_SDQ39 BG12 SB_DQ_39
DDRBD_SDQ40 BJ10 SB_DQ_40
DDRBD_SDQ41 BL9 SB_DQ_41
DDRBD_SDQ42 BK5 SB_DQ_42
DDRBD_SDQ43 BL5 SB_DQ_43
DDRBD_SDQ44 BK9 SB_DQ_44
DDRBD_SDQ45 BK10 SB_DQ_45
DDRBD_SDQ46 BJ8 SB_DQ_46
DDRBD_SDQ47 BJ6 SB_DQ_47
DDRBD_SDQ48 BF4 SB_DQ_48
DDRBD_SDQ49 BH5 SB_DQ_49
DDRBD_SDQ50 BC1 SB_DQ_50
DDRBD_SDQ51 BC2 SB_DQ_51
DDRBD_SDQ52 BK3 SB_DQ_52
DDRBD_SDQ53 BE4 SB_DQ_53
DDRBD_SDQ54 BD3 SB_DQ_54
DDRBD_SDQ55 BJ2 SB_DQ_55
DDRBD_SDQ56 BA3 SB_DQ_56
DDRBD_SDQ57 BB3 SB_DQ_57
DDRBD_SDQ58 AR1 SB_DQ_58
DDRBD_SDQ59 AT3 SB_DQ_59
DDRBD_SDQ60 AY2 SB_DQ_60
DDRBD_SDQ61 AY3 SB_DQ_61
DDRBD_SDQ62 AU2 SB_DQ_62
DDRBD_SDQ63 AT2 SB_DQ_63

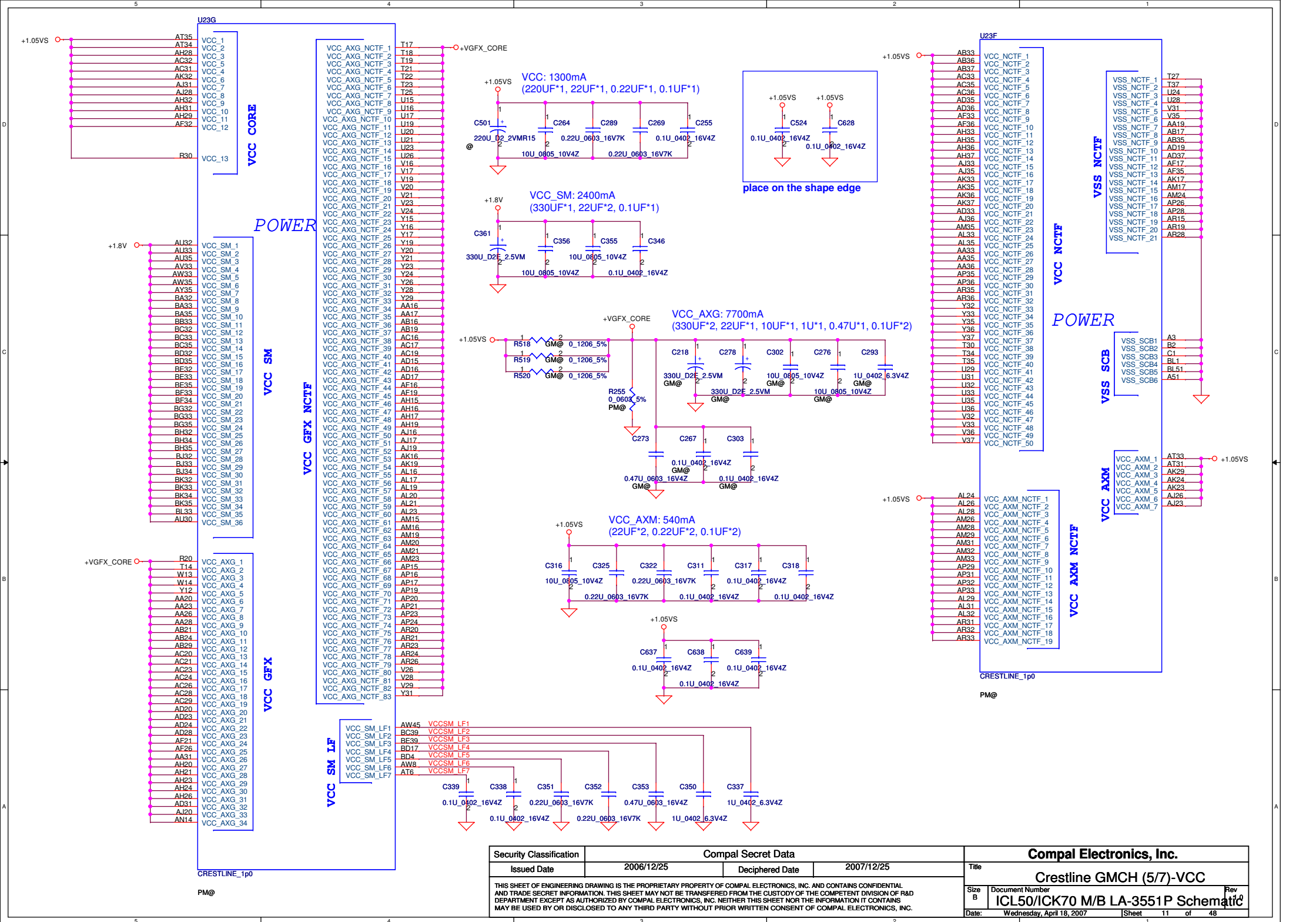
DDR SYSTEM MEMORY B

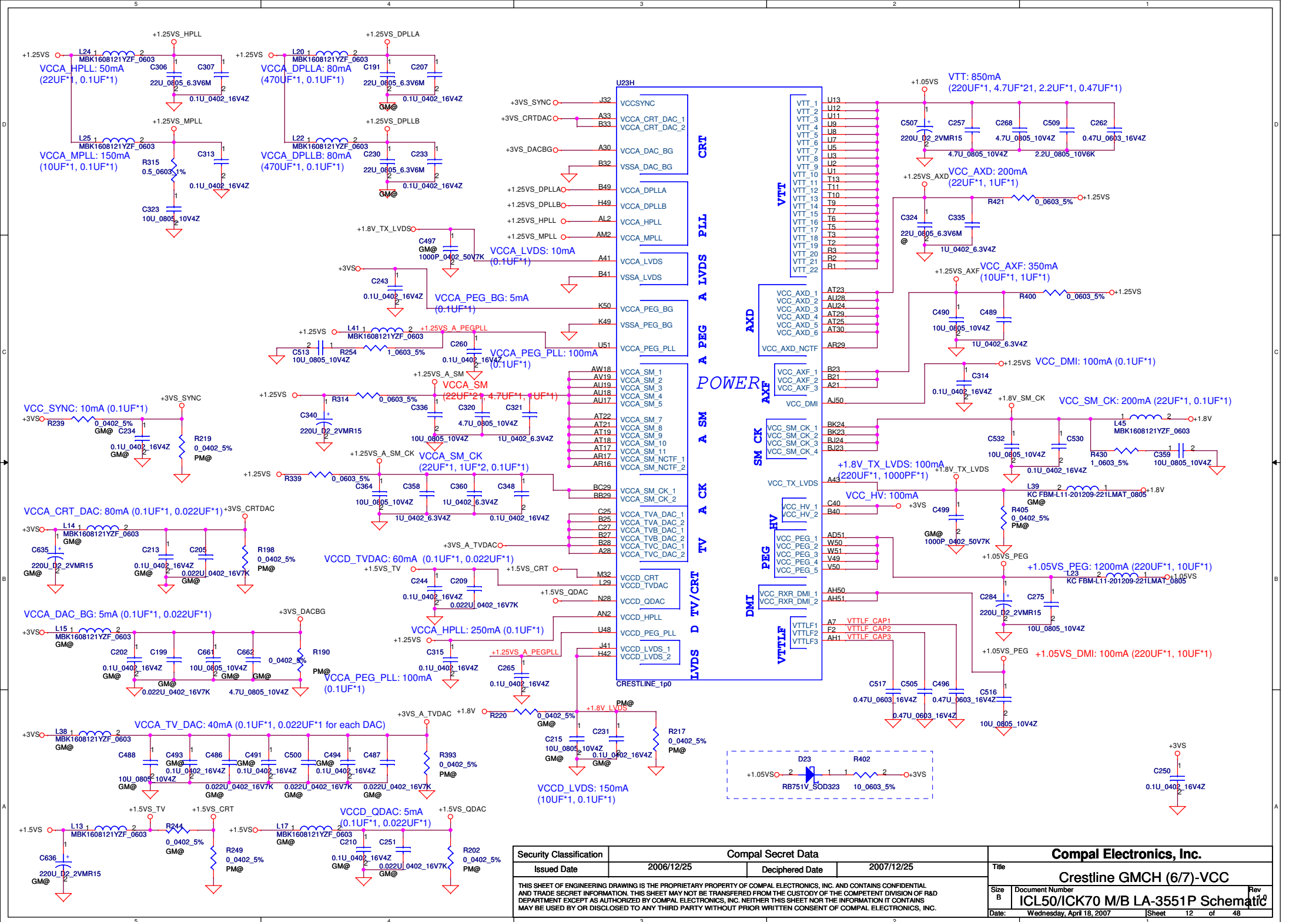
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SB_BS_1 BG18 <== DDRB_SBS1# 15
SB_BS_2 BG36 <== DDRB_SBS2# 15
SB_CAS# BE17 <== DDRB_SCAS# 15
SB_DM_0 AR50 <== DDRB_SDM0
SB_DM_1 BD49 <== DDRB_SDM1
SB_DM_2 BK45 <== DDRB_SDM2
SB_DM_3 BL39 <== DDRB_SDM3
SB_DM_4 BH12 <== DDRB_SDM4
SB_DM_5 BJ7 <== DDRB_SDM5
SB_DM_6 BE3 <== DDRB_SDM6
SB_DM_7 AW2 <== DDRB_SDM7
SB_DQS_0 AT50 <== DDRB_SDQS0
SB_DQS_1 BD50 <== DDRB_SDQS1
SB_DQS_2 BK46 <== DDRB_SDQS2
SB_DQS_3 BK39 <== DDRB_SDQS3
SB_DQS_4 BJ12 <== DDRB_SDQS4
SB_DQS_5 BL7 <== DDRB_SDQS5
SB_DQS_6 BE2 <== DDRB_SDQS6
SB_DQS_7 AV2 <== DDRB_SDQS7
SB_DQS#_0 AU50 <== DDRB_SDQS0#
SB_DQS#_1 BC50 <== DDRB_SDQS1#
SB_DQS#_2 BL45 <== DDRB_SDQS2#
SB_DQS#_3 BK38 <== DDRB_SDQS3#
SB_DQS#_4 BK12 <== DDRB_SDQS4#
SB_DQS#_5 BK7 <== DDRB_SDQS5#
SB_DQS#_6 BE2 <== DDRB_SDQS6#
SB_DQS#_7 AV3 <== DDRB_SDQS7#
SB_MA_0 BC18 <== DDRB_SMA0
SB_MA_1 BG28 <== DDRB_SMA1
SB_MA_2 BG25 <== DDRB_SMA2
SB_MA_3 AW17 <== DDRB_SMA3
SB_MA_4 BE25 <== DDRB_SMA4
SB_MA_5 BA29 <== DDRB_SMA5
SB_MA_6 BC28 <== DDRB_SMA6
SB_MA_7 AY28 <== DDRB_SMA7
SB_MA_8 BD37 <== DDRB_SMA8
SB_MA_9 BG17 <== DDRB_SMA9
SB_MA_10 BE37 <== DDRB_SMA10
SB_MA_11 BA39 <== DDRB_SMA11
SB_MA_12 BG13 <== DDRB_SMA12
SB_MA_13
SB_RAS# AV16 <== DDRB_SRAS# 15
SB_RCVEN# AY18 <== DDRB_SRCVEN# PAD T14
SB_WE# BC17 <== DDRB_SWE# 15

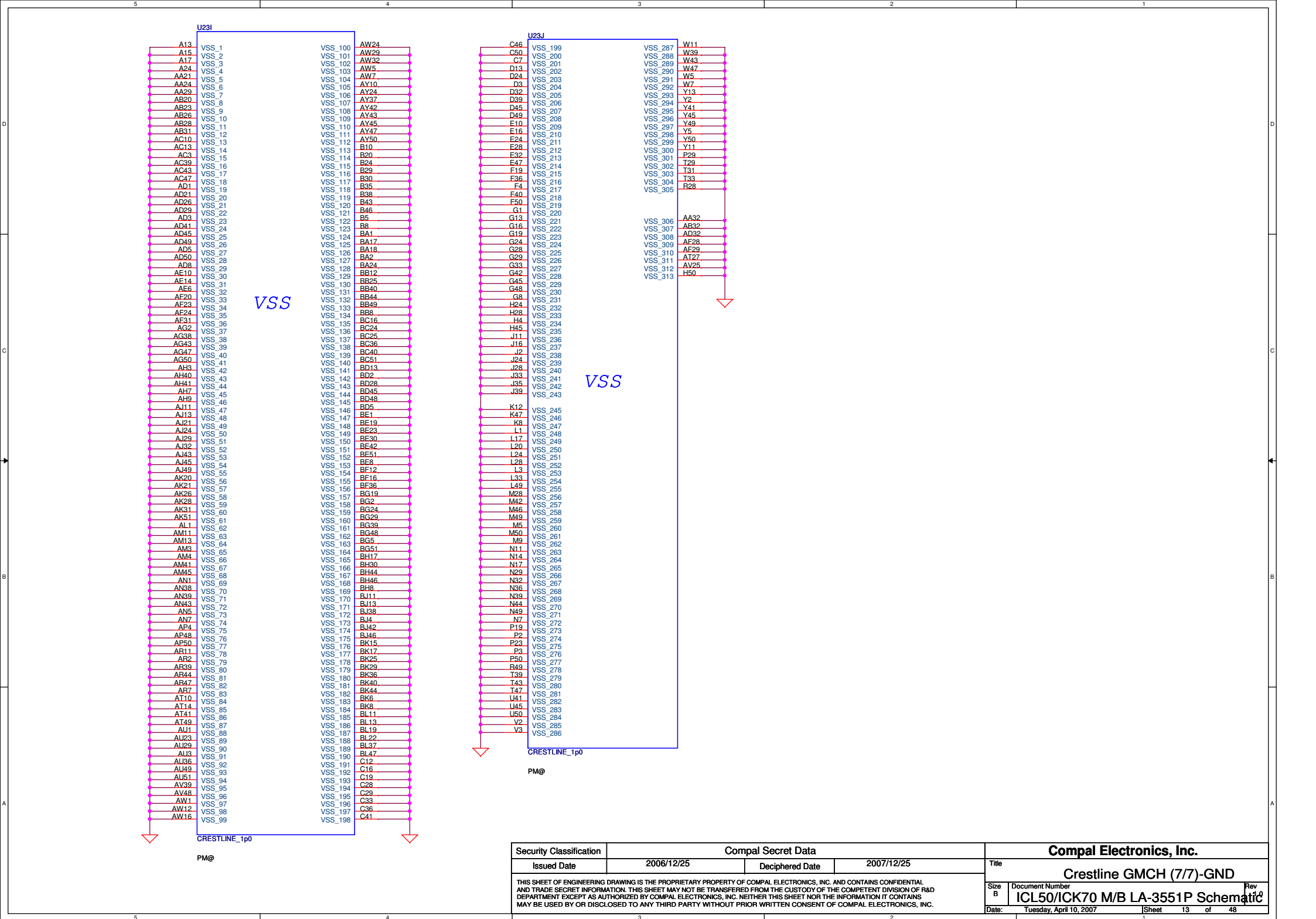
CRESTLINE_1p0

PM@

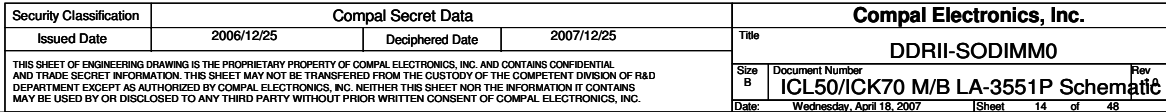
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				Date:	Tuesday, April 10, 2007
				Sheet	9 of 48
				Crestline GMCH (3/7)-DDRII	
				ICL50/ICK70 M/B LA-3551P Schematic	
				Rev	







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		Size B	Document Number						Rev
		ICL50/ICK700 M/B LA-3551P Schematic						0	
Date:		Tuesday, April 10, 2007		Sheet		13		of 48	

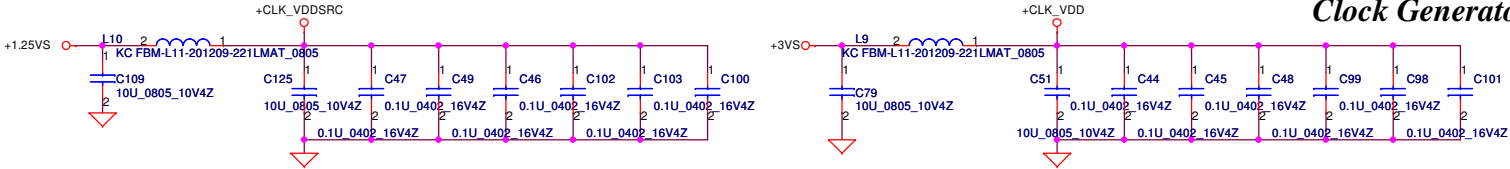
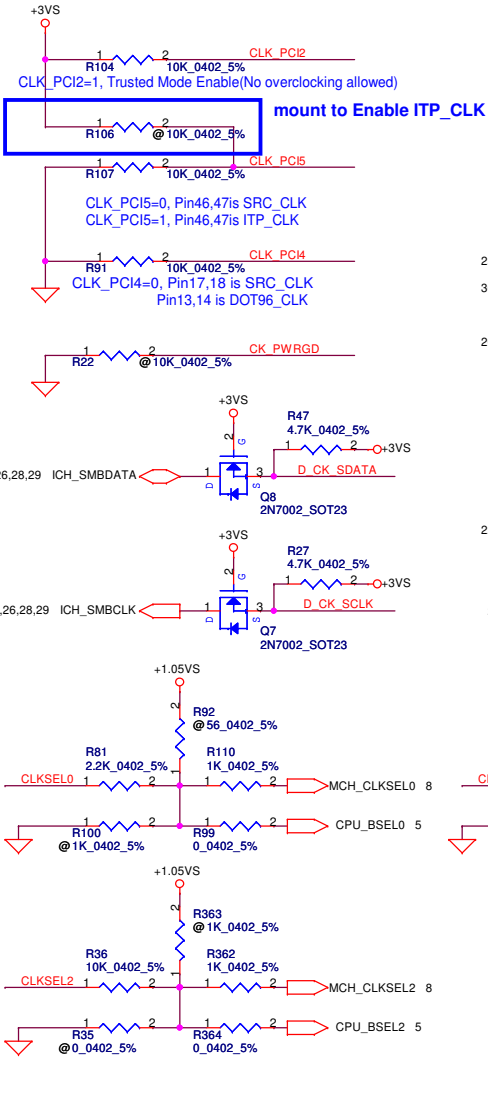


FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

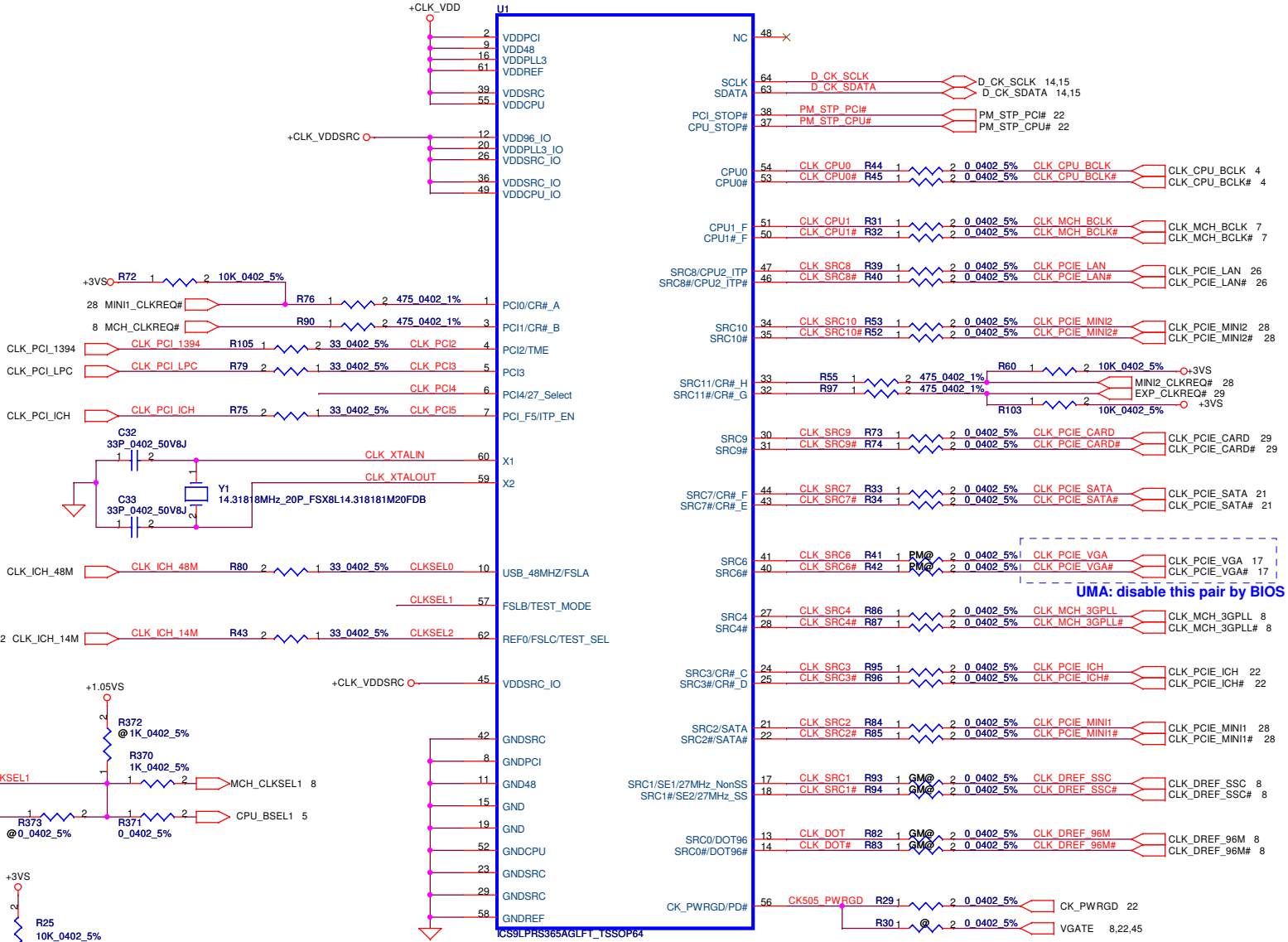
Table : IC59LPR365

CLK_REQ#	Control	Free-Run
CR#_A(WLAN)	PCIEX2	PCIEX0
CR#_B(MCH)	PCIEX4	PCIEX1
CR#_G(NEW CARD)	PCIEX9	
CR#_H(MINI CARDII)	PCIEX10	

SRC6(VGA_CLK): Discrete VGA[Enable] UMA[Disable]



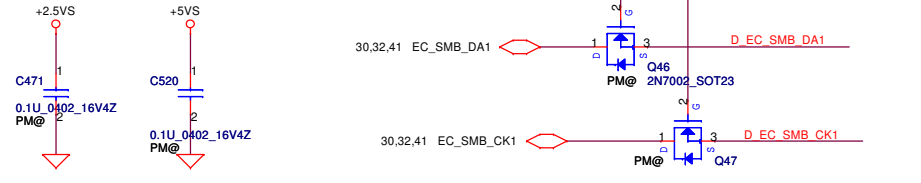
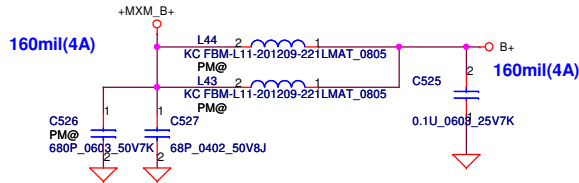
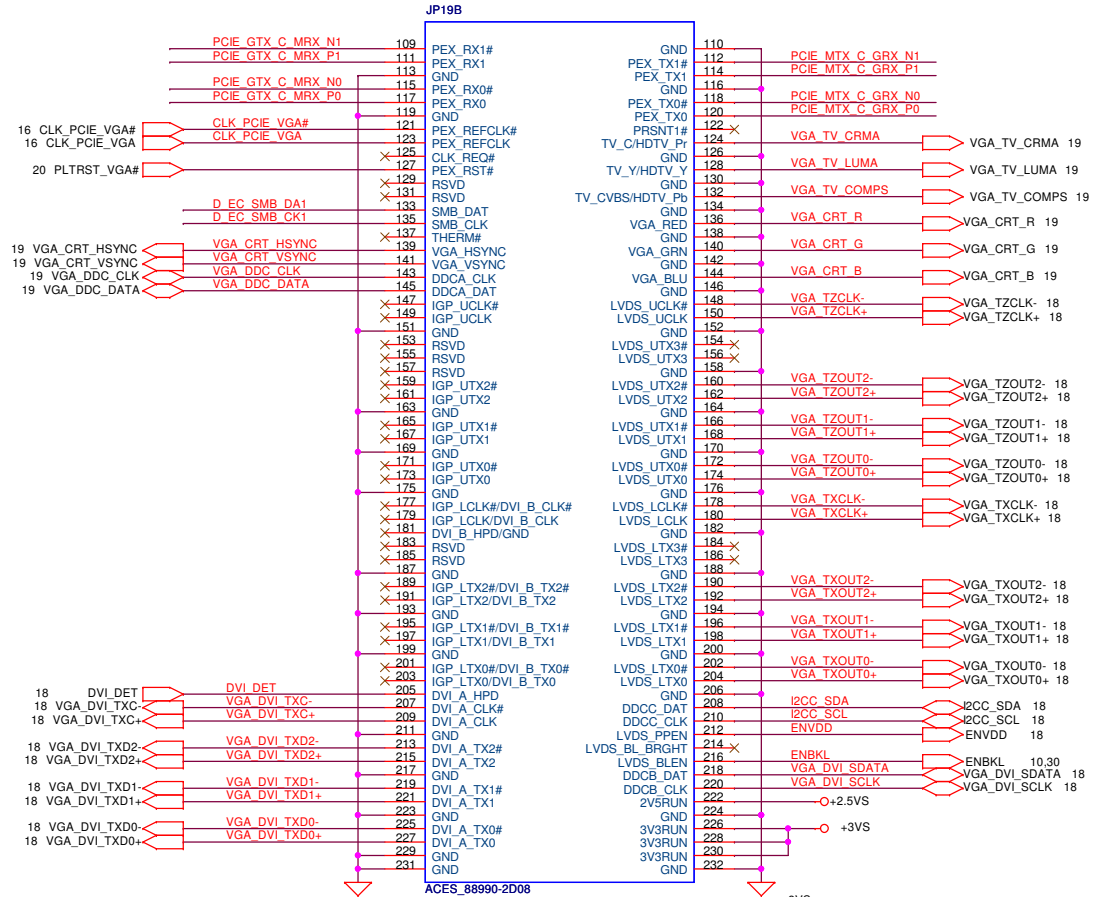
Clock Generator



UMA: disable this pair by BIOS

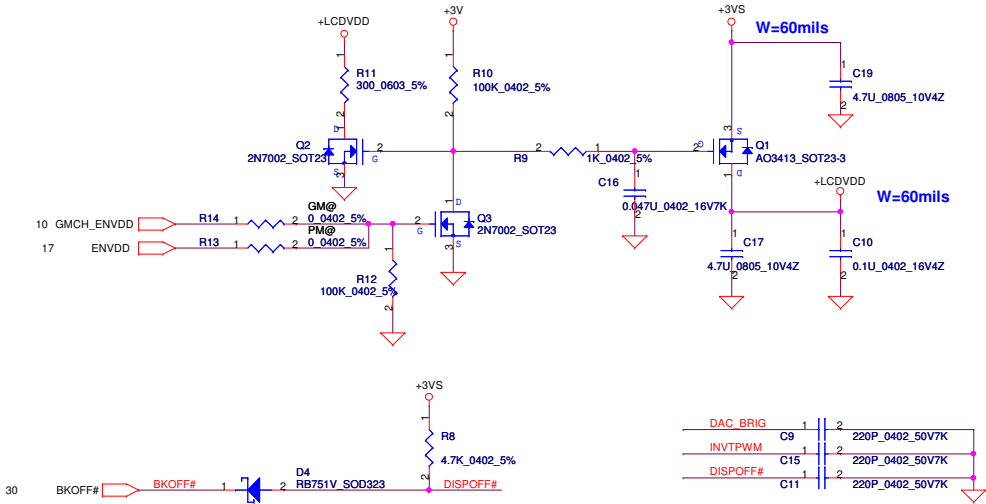
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/12/25	Deciphered Date	2007/12/25	Title	
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Size	Document Number	Rev		Date	
B	ICL50/ICK70 M/B LA-3551P Schematic	1		Wednesday, April 18, 2007	
Sheet		16		of 48	

10 PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_P[0..15]
10 PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
10 PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_P[0..15]
10 PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

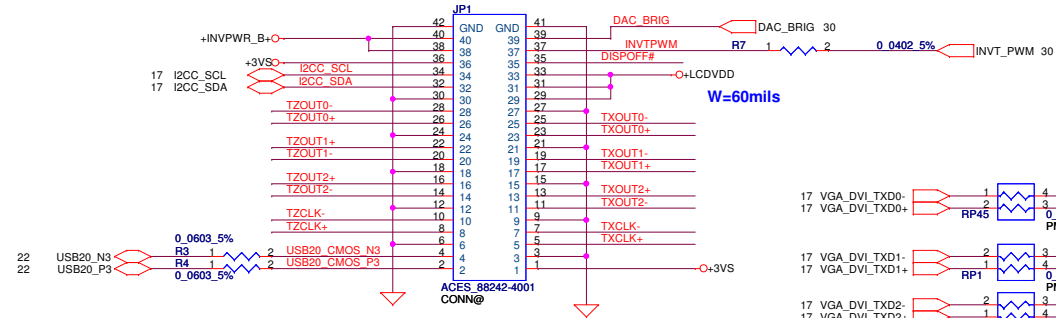


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				ICL50/ICK70 M/B LA-3551P Schematic		
				Date:	Wednesday, April 18, 2007	Sheet

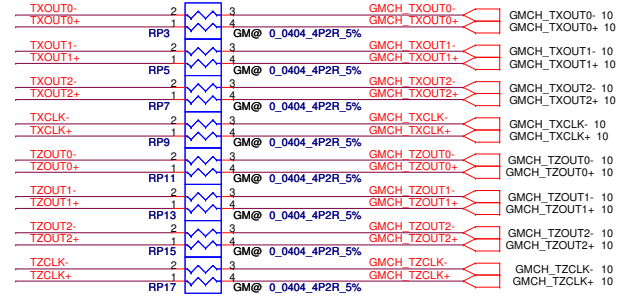
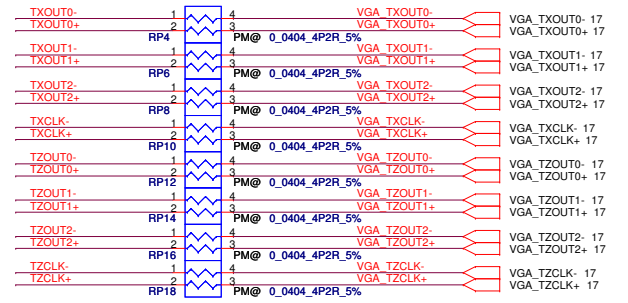
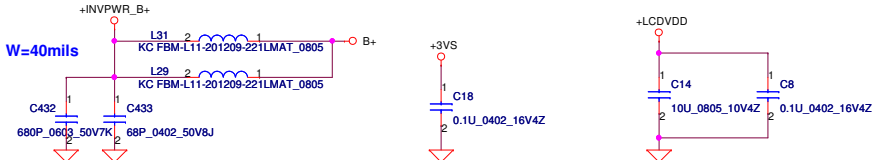
LCD POWER CIRCUIT



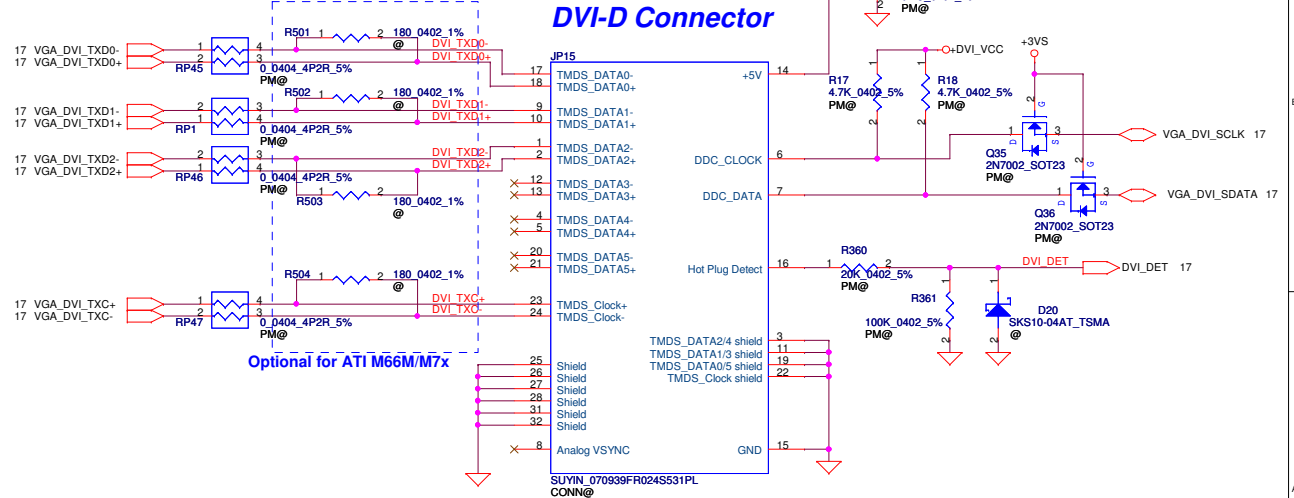
LCD/PANEL BD. Conn.



For GMCH DPST

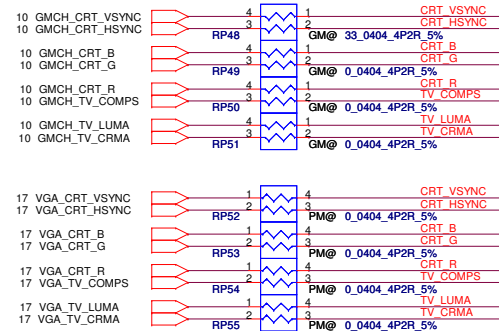


DVI-D Connector



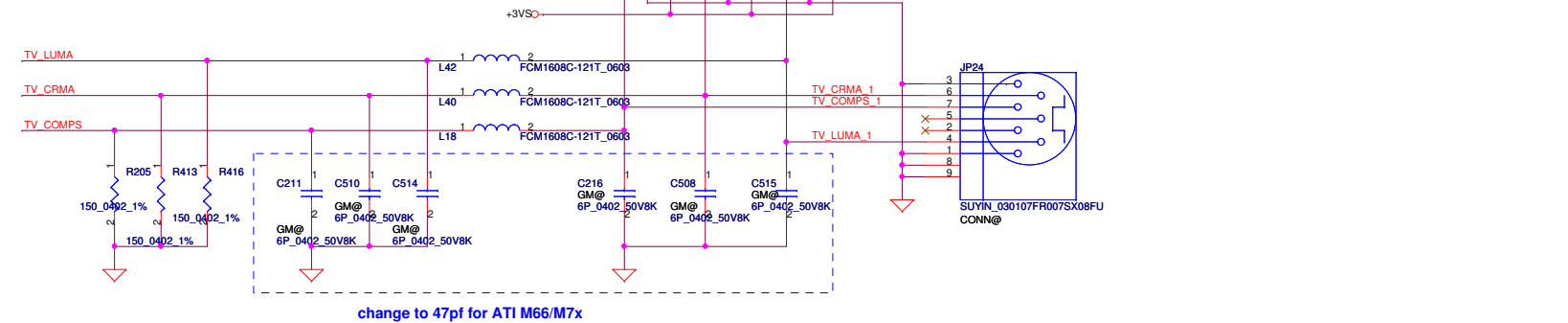
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/12/25				Title			
Deciphered Date				2007/12/25				LVDS & DVI Connector			
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				ICL50/ICK70 M/B LA-3551P Schematic				Rev			
				Date: Wednesday, April 18, 2007				Sheet 18 of 48			

CRT Connector

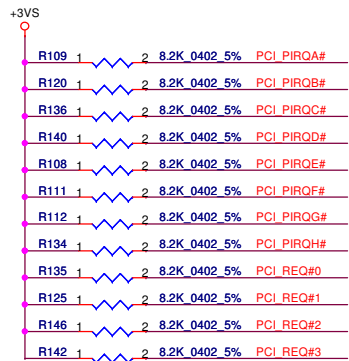
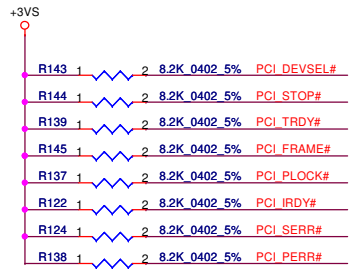


Place closed to chipset

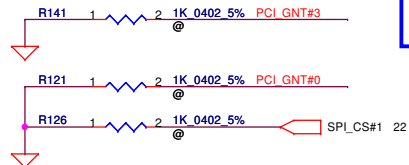
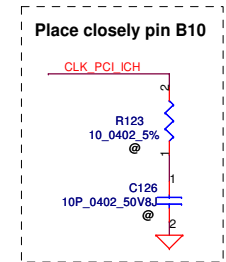
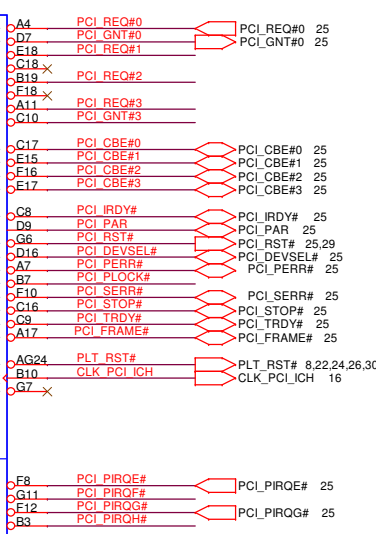
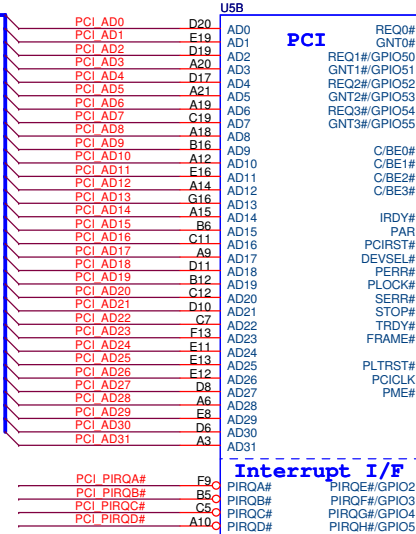
TV-OUT Conn.



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				ICL50/ICK70 M/B LA-3551P Schematic	
				Date	Wednesday, April 18, 2007
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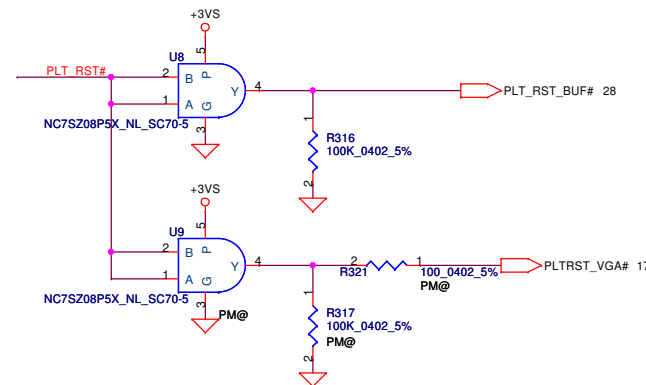


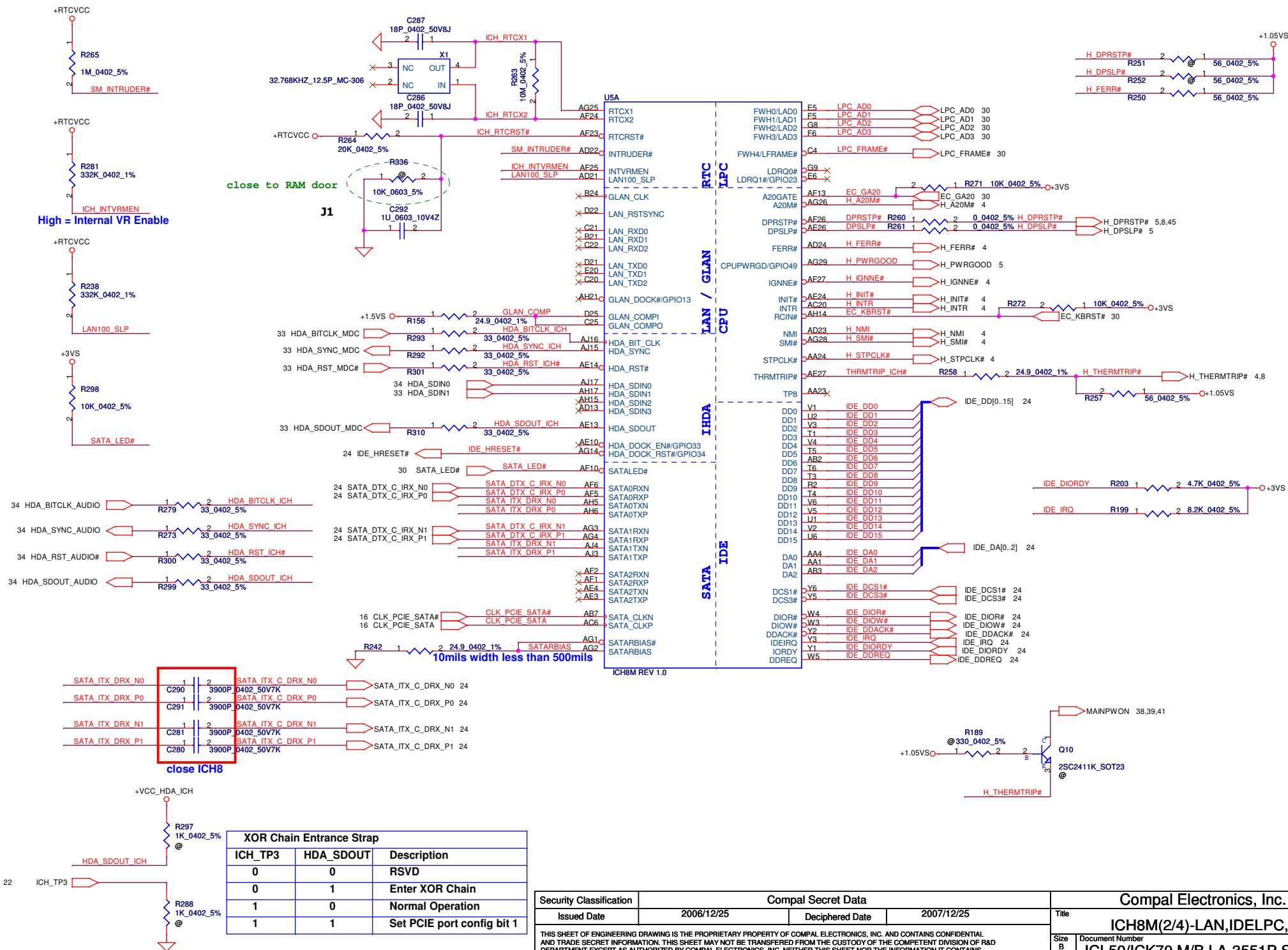
25 PCI_AD[0..31]

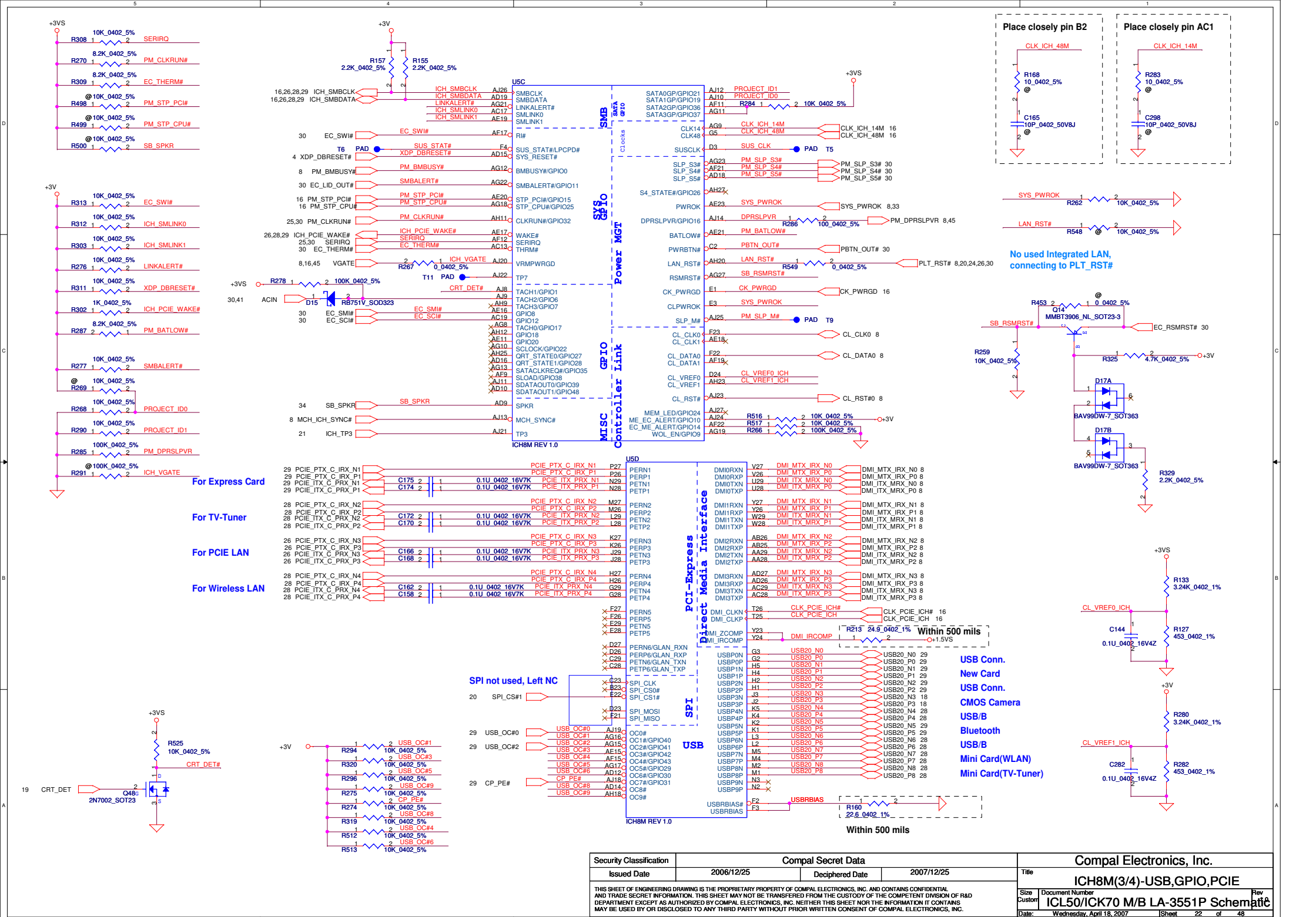


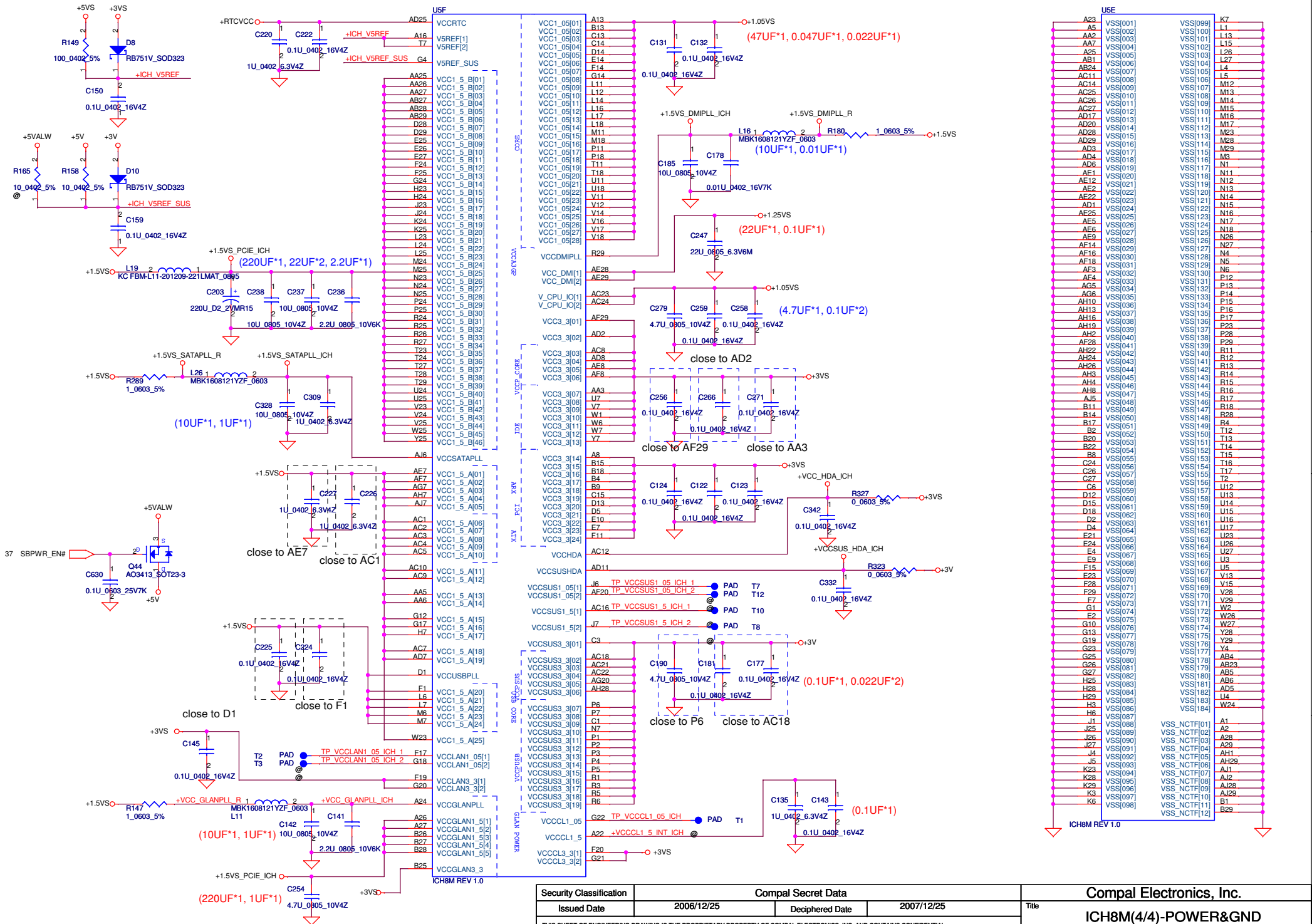
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

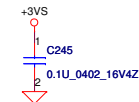
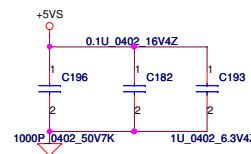
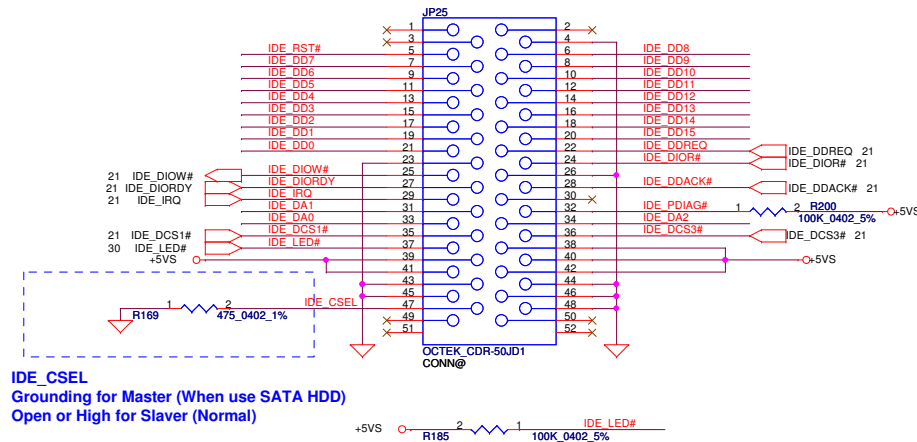
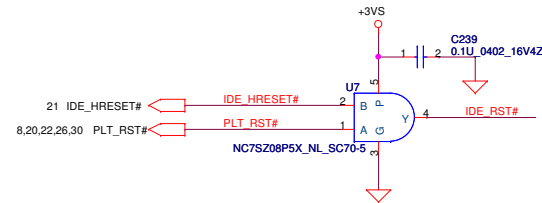
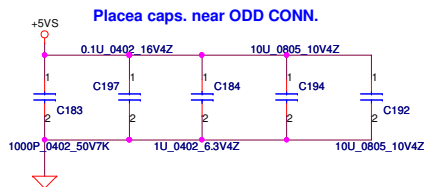
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



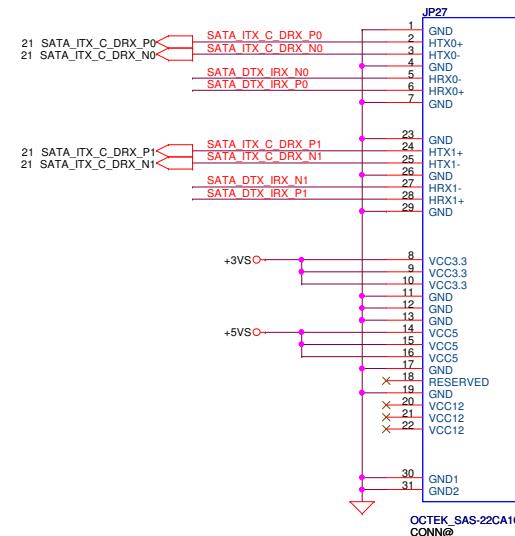
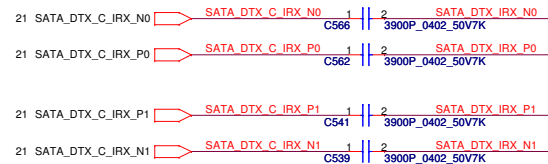




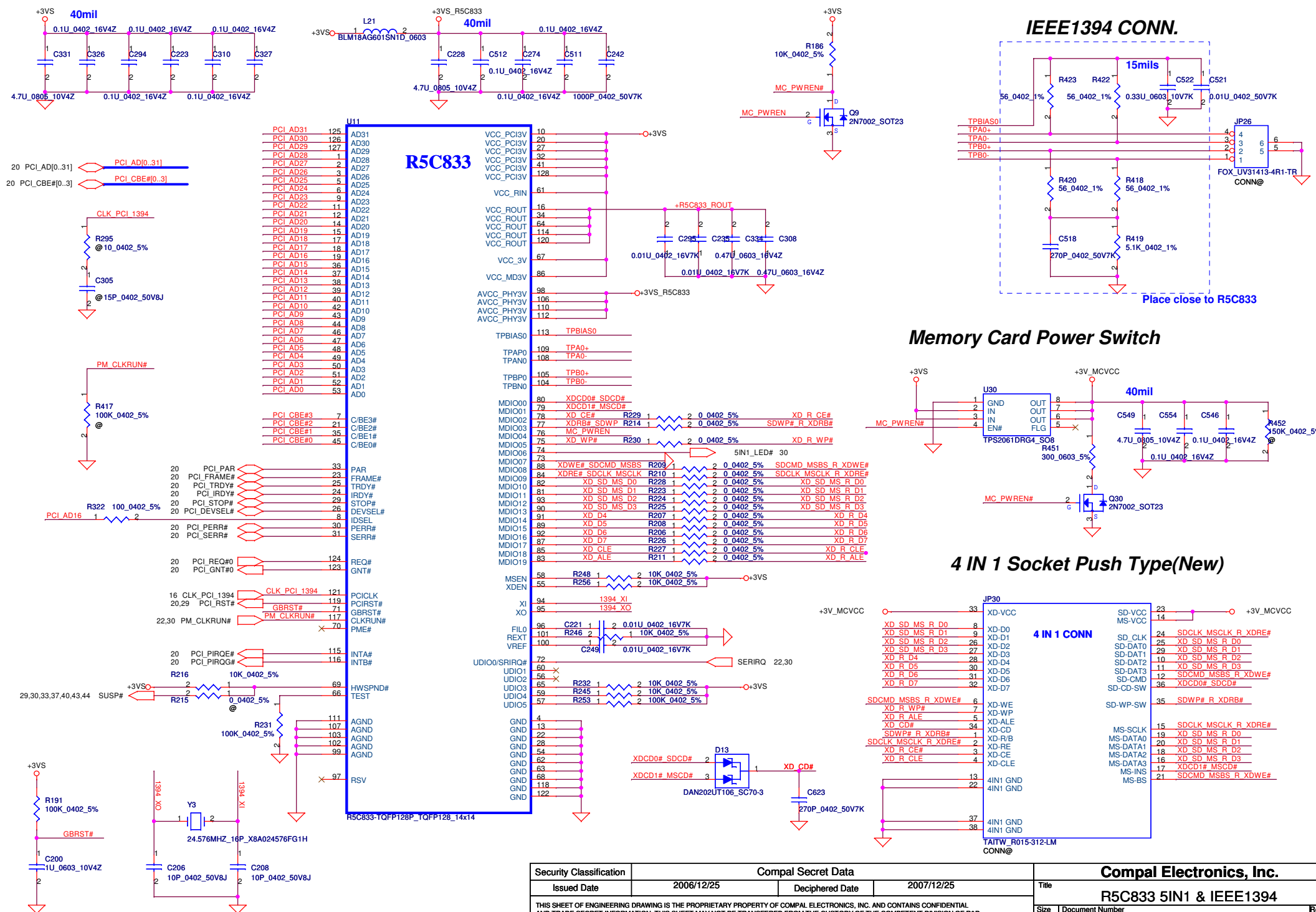




SATA HDD Conn.(SAS Connector)

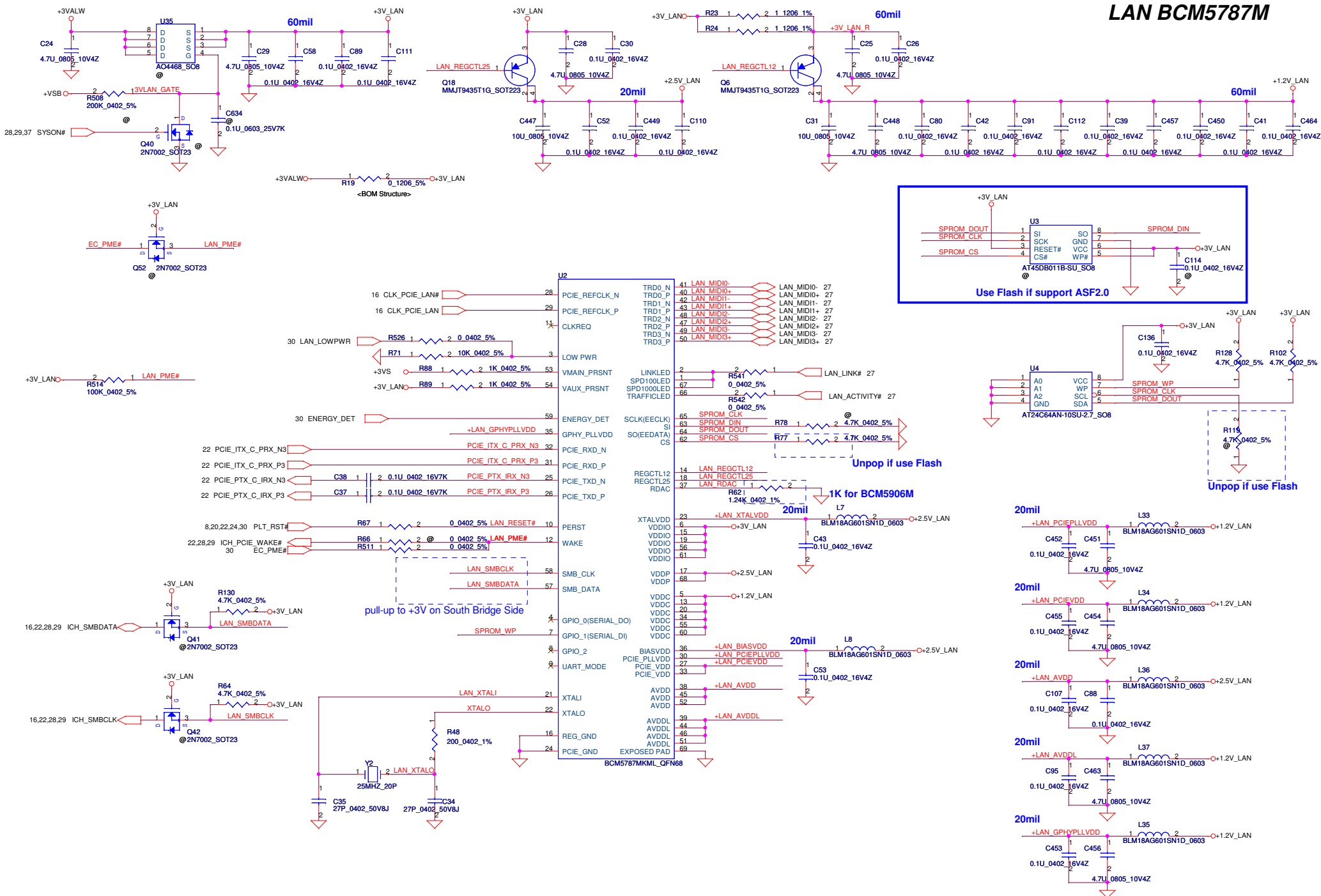


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						Size B		Document Number		Rev	
						ICL50/ICK70 M/B LA-3551P Schematic					
						Date: Tuesday, April 10, 2007		Sheet 24 of 48			

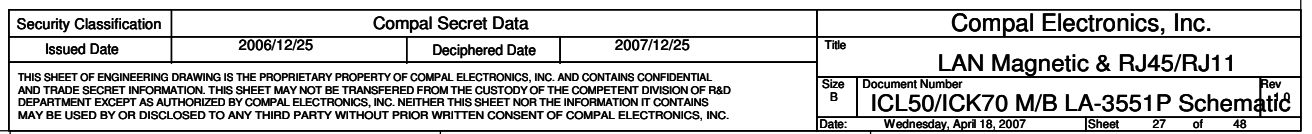


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								Size	B	Document Number	ICL50/ICK70 M/B LA-3551P Schematic		Rev	1
								Date:	Wednesday, April 18, 2007		Sheet	25	of	48

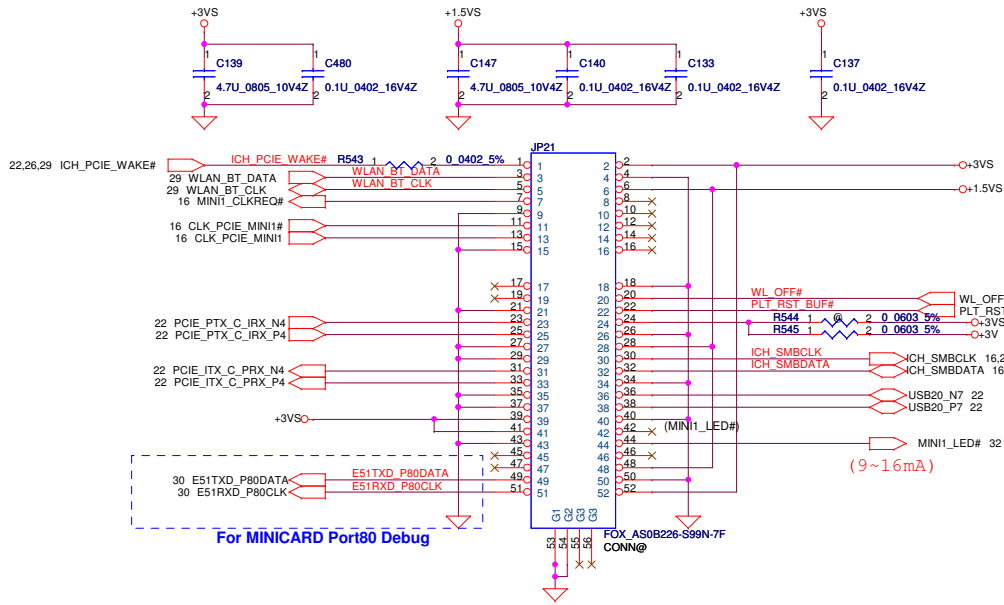
LAN BCM5787M



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								LAN BCM5787M	
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						B			
						Document Number		ICL50/ICK70 M/B LA-3551P Schematic	
						Date:		Wednesday, April 18, 2007	
						Sheet		26 of 48	



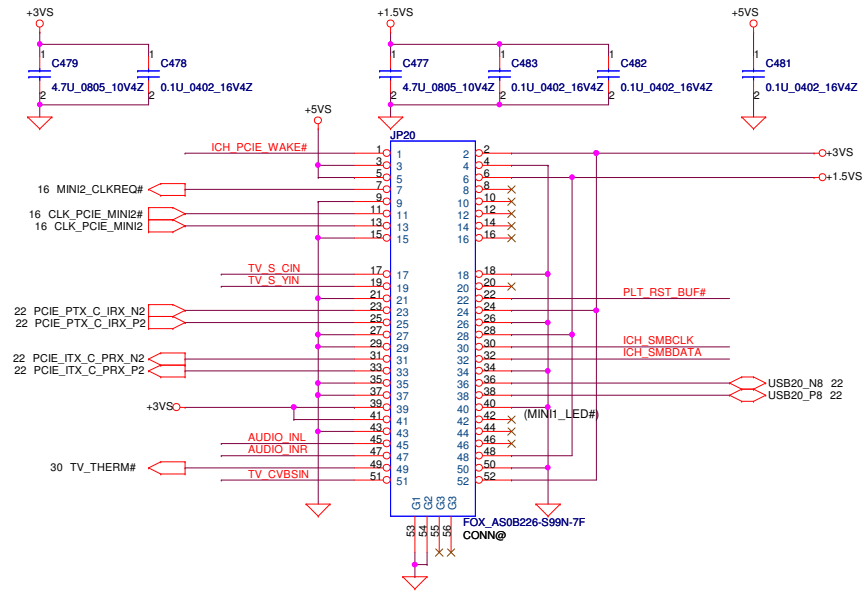
For Wireless LAN



Mini Card Power Rating

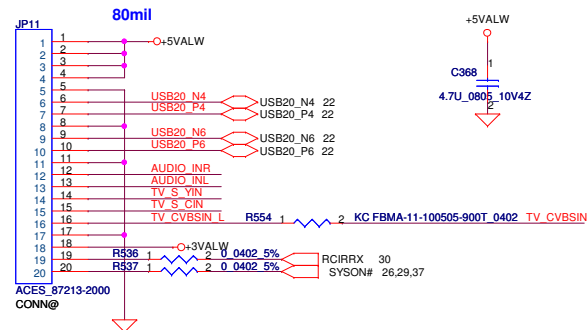
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For TV-Tuner/HW MPEG

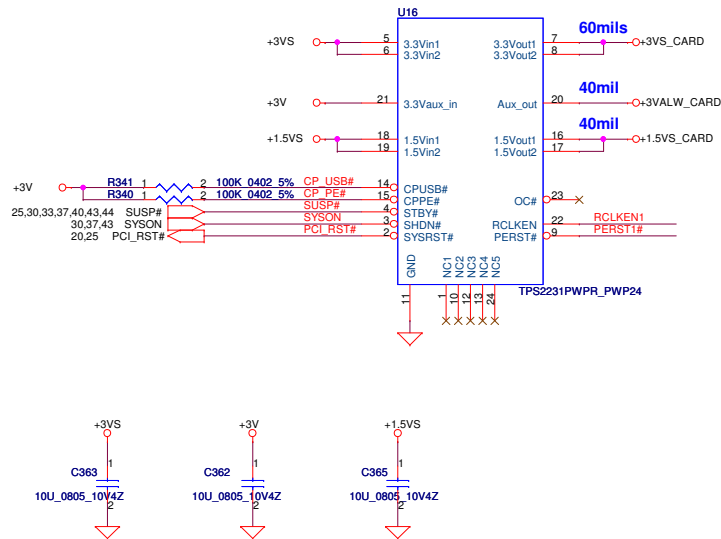


To USB/B Connector

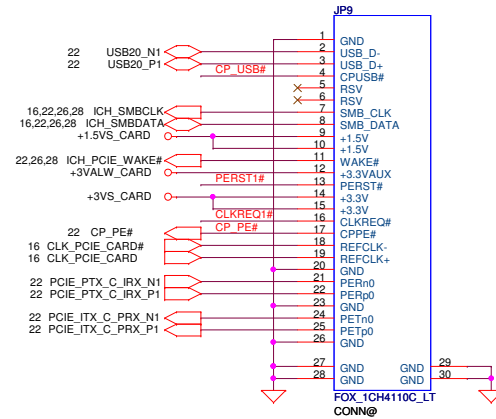
AV-IN Connector
CIR



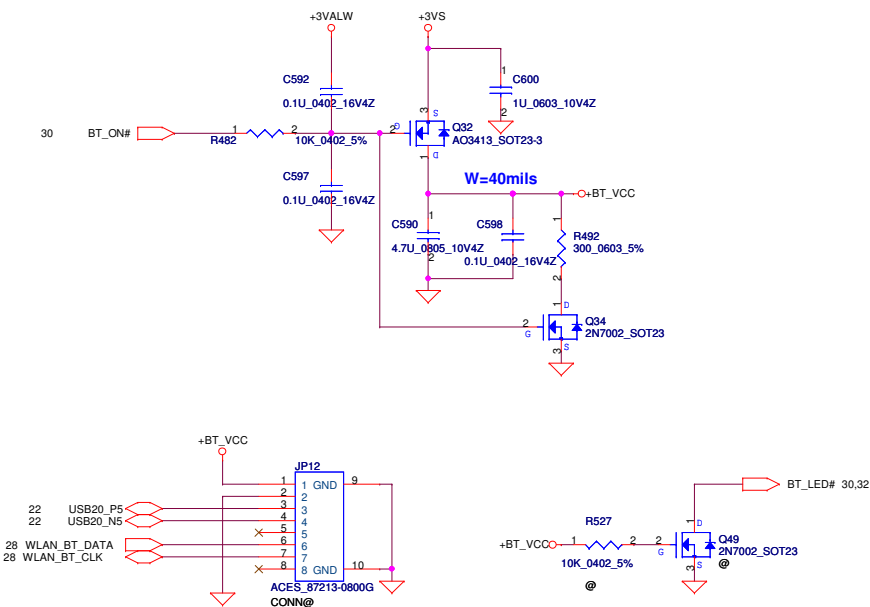
New Card Power Switch



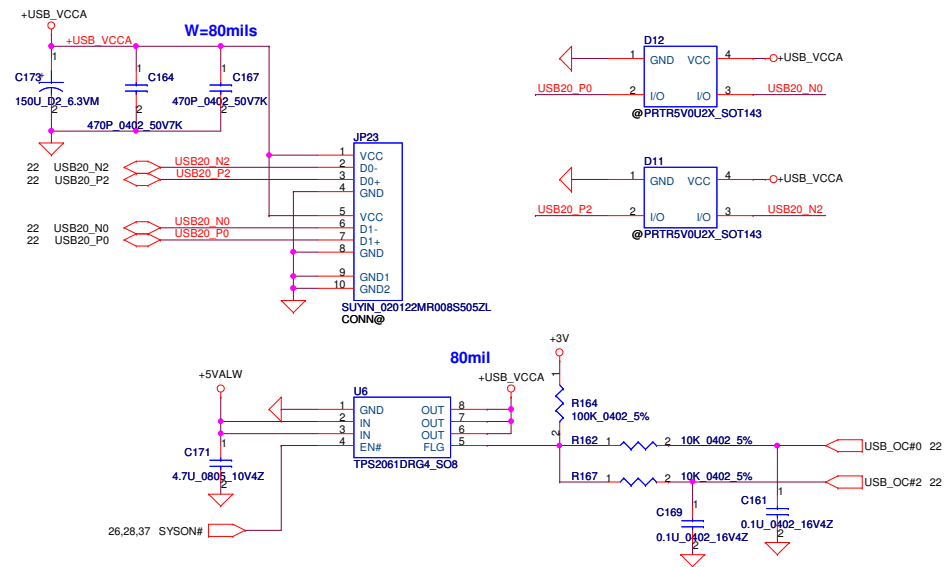
New Card Socket (Left/TOP)



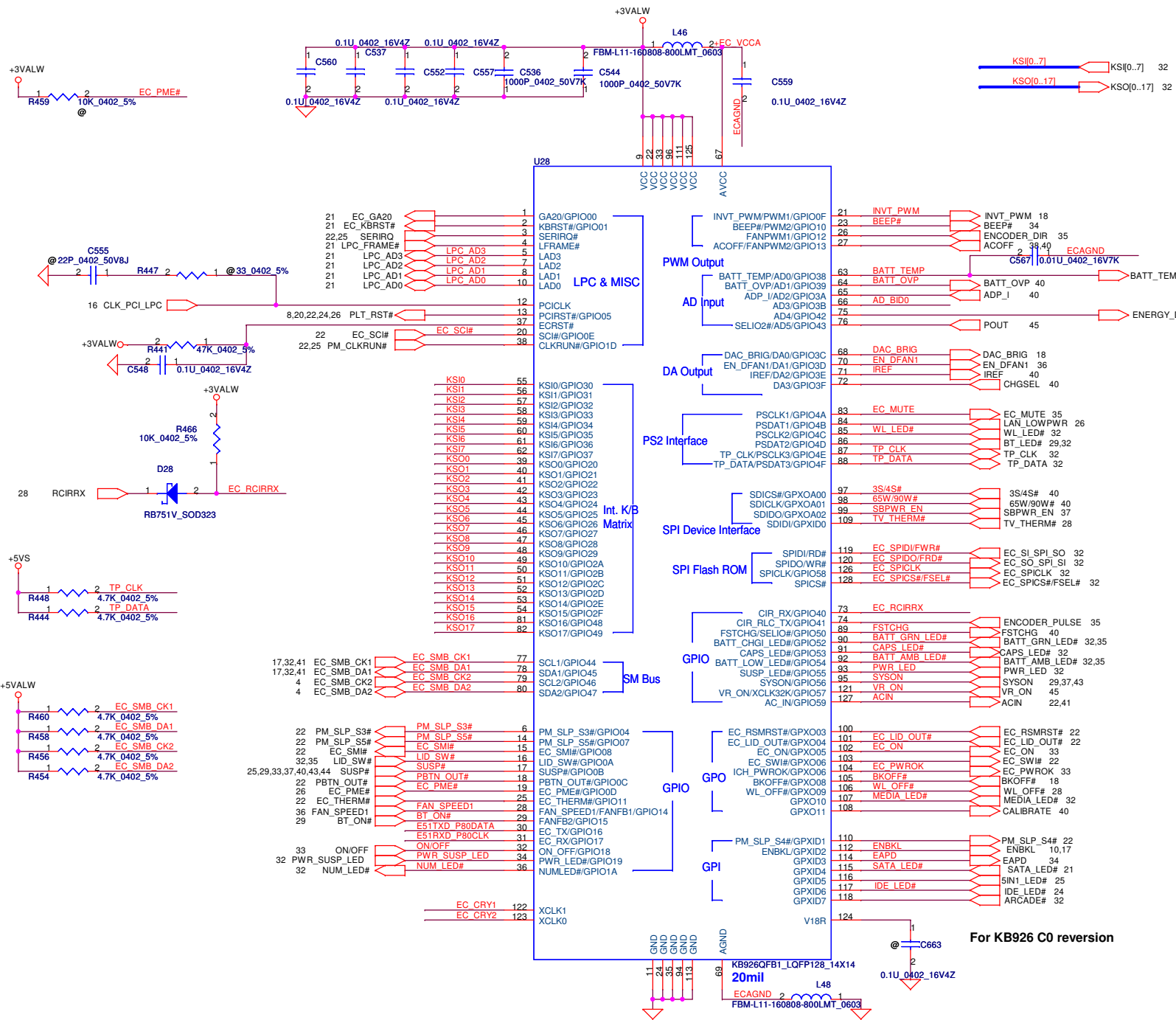
Bluetooth Conn.



USB CONN. (Stack-up Type)

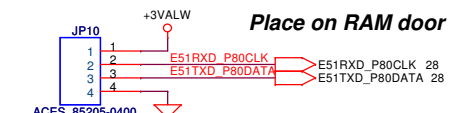


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Size B	Document Number	ICL50/ICK70 M/B LA-3551P Schematic		Rev	
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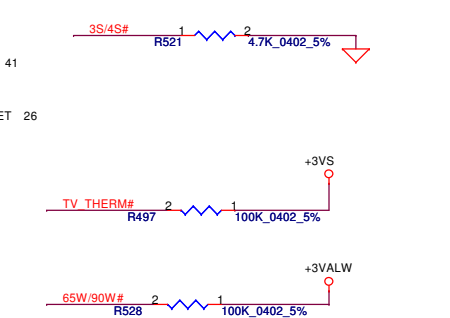
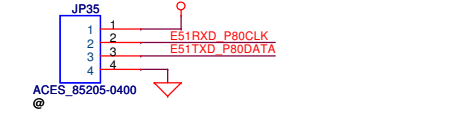


For EC Tools

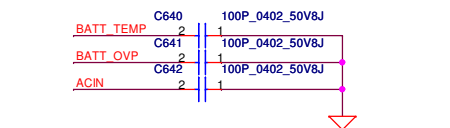
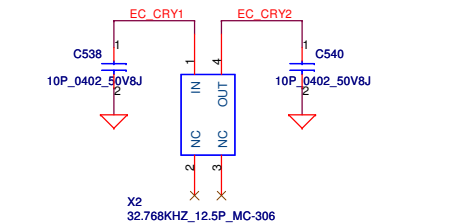
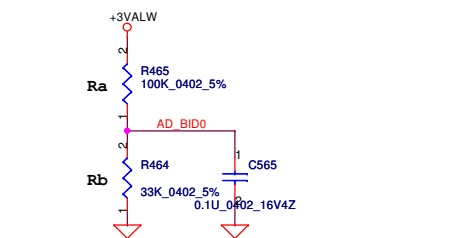
Place on RAM door



Place on MiniCard

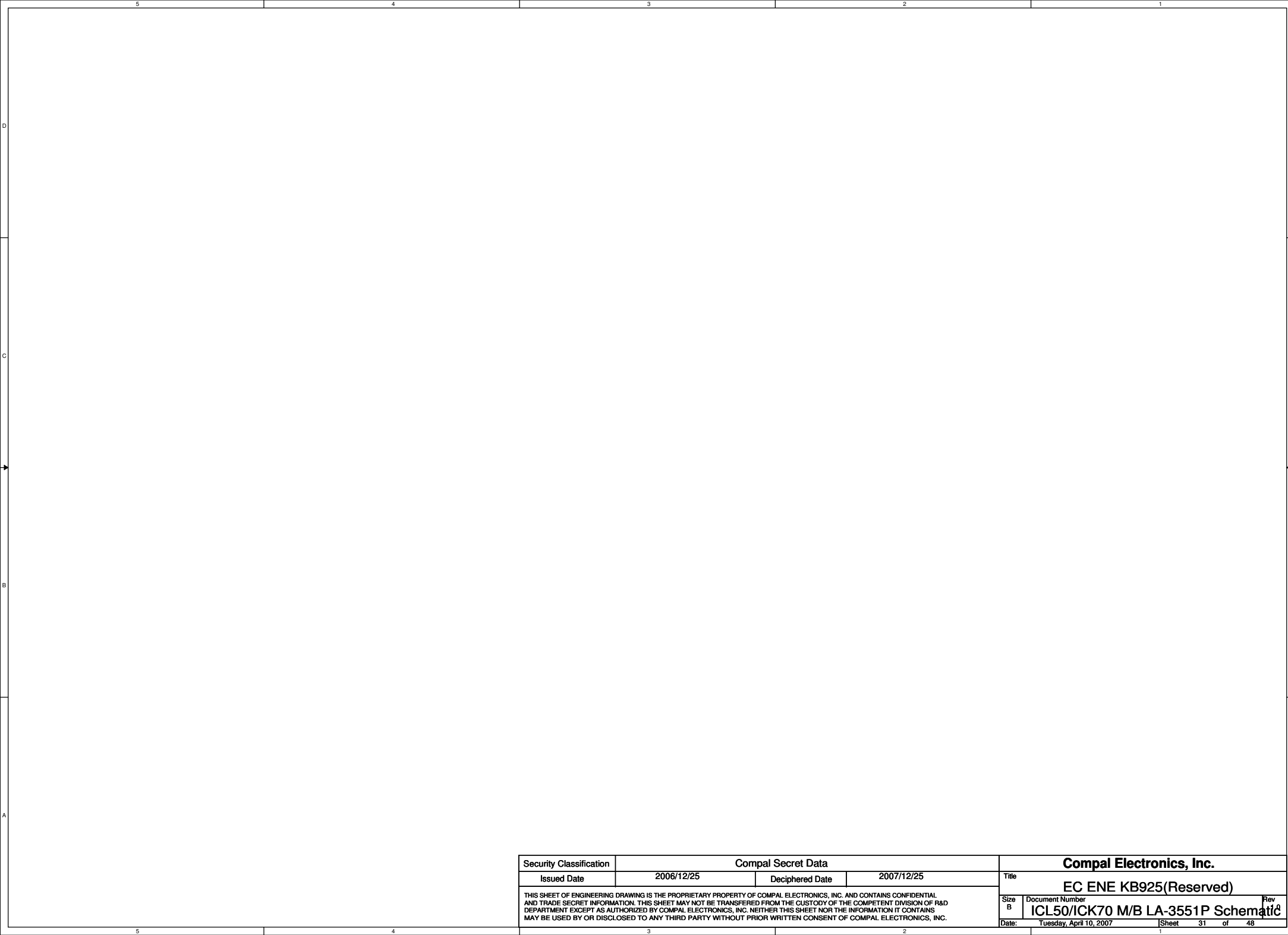


Analog Board ID definition, Please see page 3.

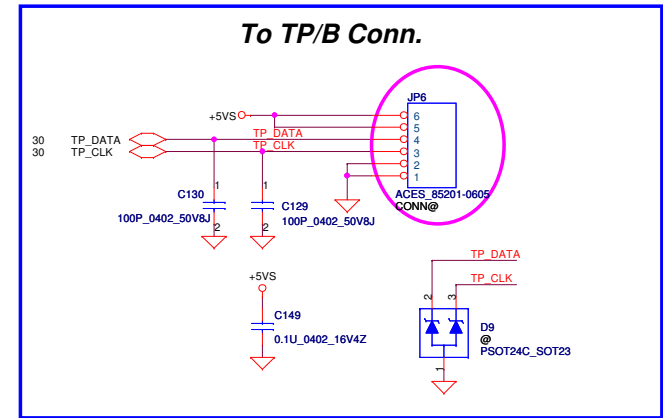
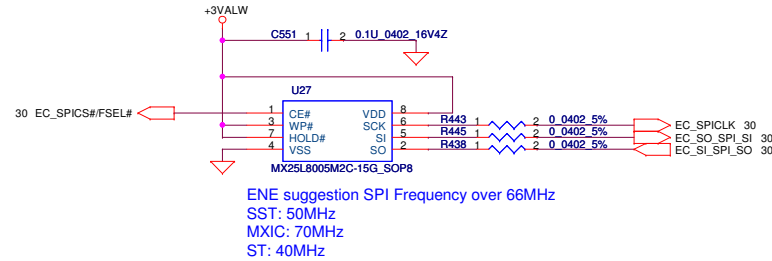
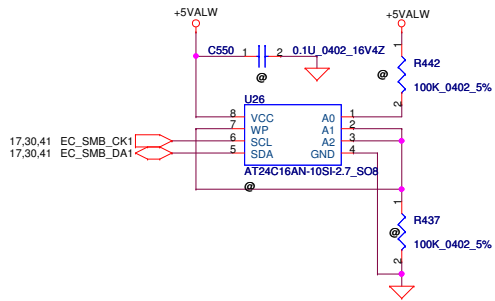


For KB926 C0 reversion

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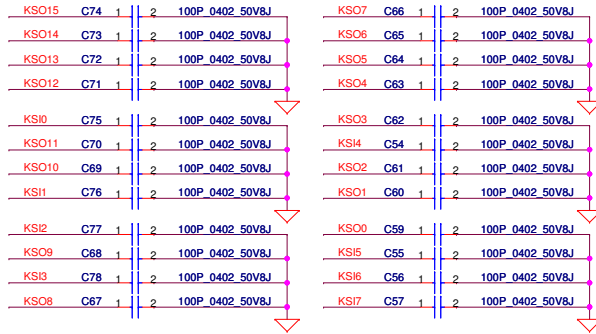
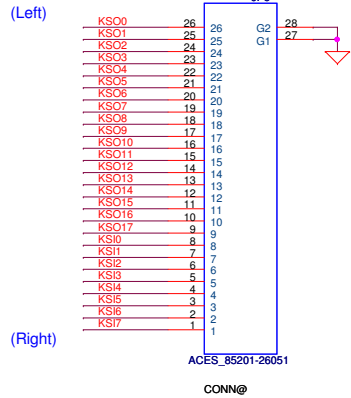


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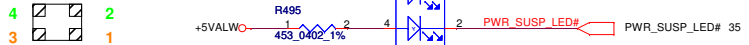


INT_KBD Conn.

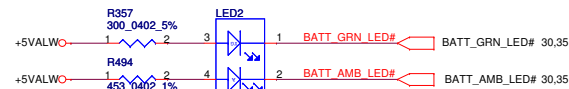
KSII[0..7] 30
KSO[0..17] 30



Compal Footprint

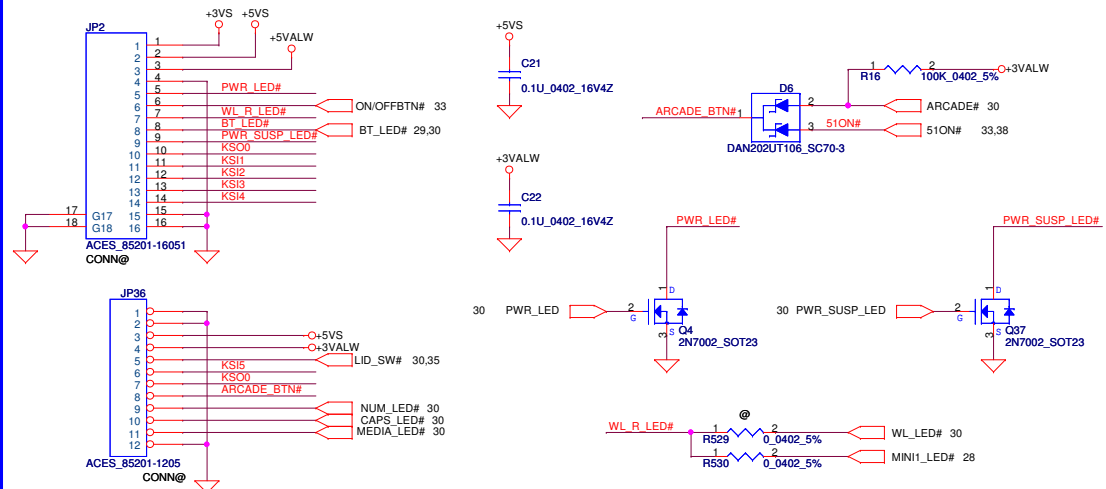


HT-297DQ/GQ_AMB/YG_0603

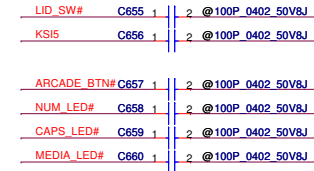
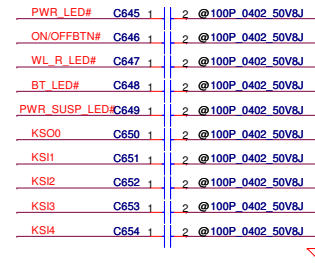


HT-297DQ/GQ_AMB/YG_0603

To BTN/B Conn.



	KSO0
KSII1	WL_BTN#
KSII2	BT_BTN#
KSII3	EMAIL_BTN#
KSII4	IE_BTN#
KSII5	E-KEY_BTN#

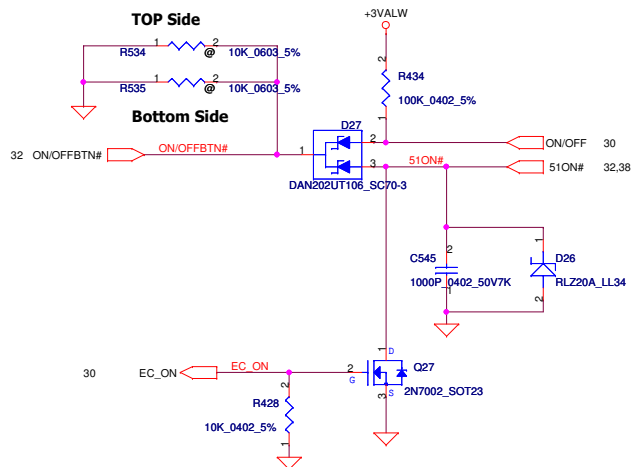


FOR EMI

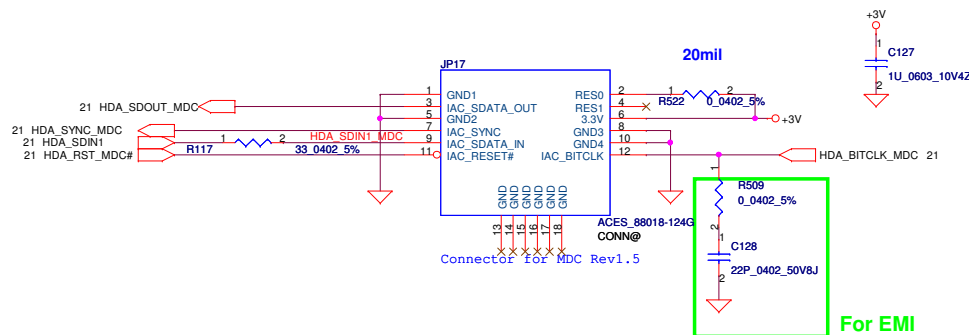
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				Date: Wednesday, April 18, 2007	Sheet 32 of 48
				BIOS, I/O Port & K/B Connector	
				ICL50/ICK70 M/B LA-3551P Schematic	

Power Button

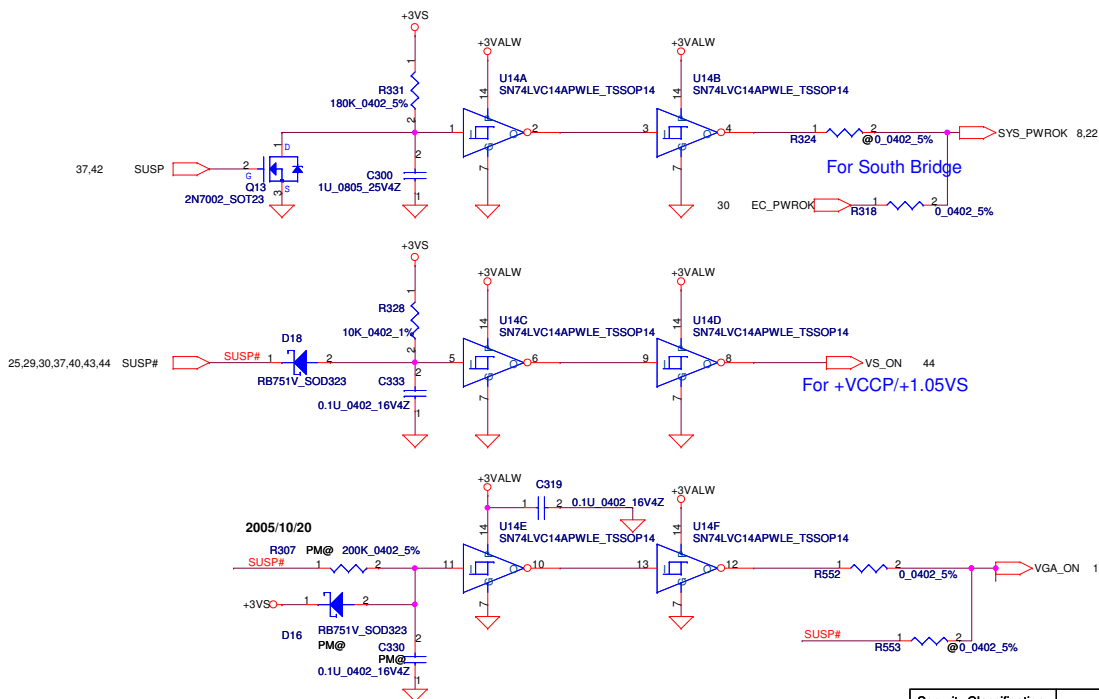
ON/OFF switch



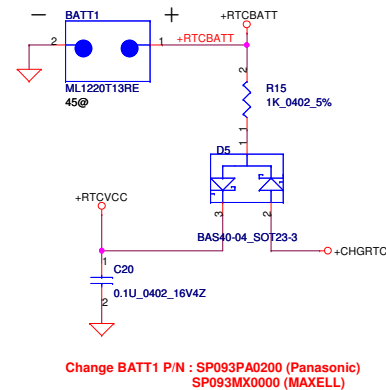
HDA MDC Conn.



Power ON Circuit

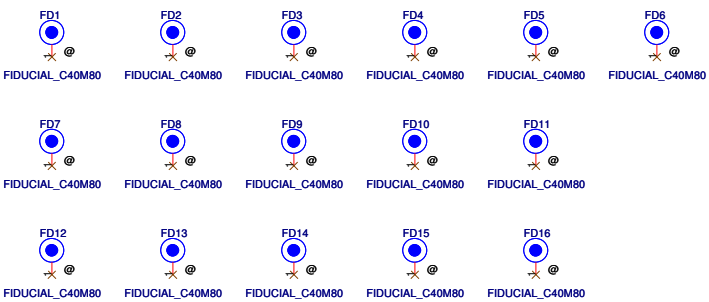
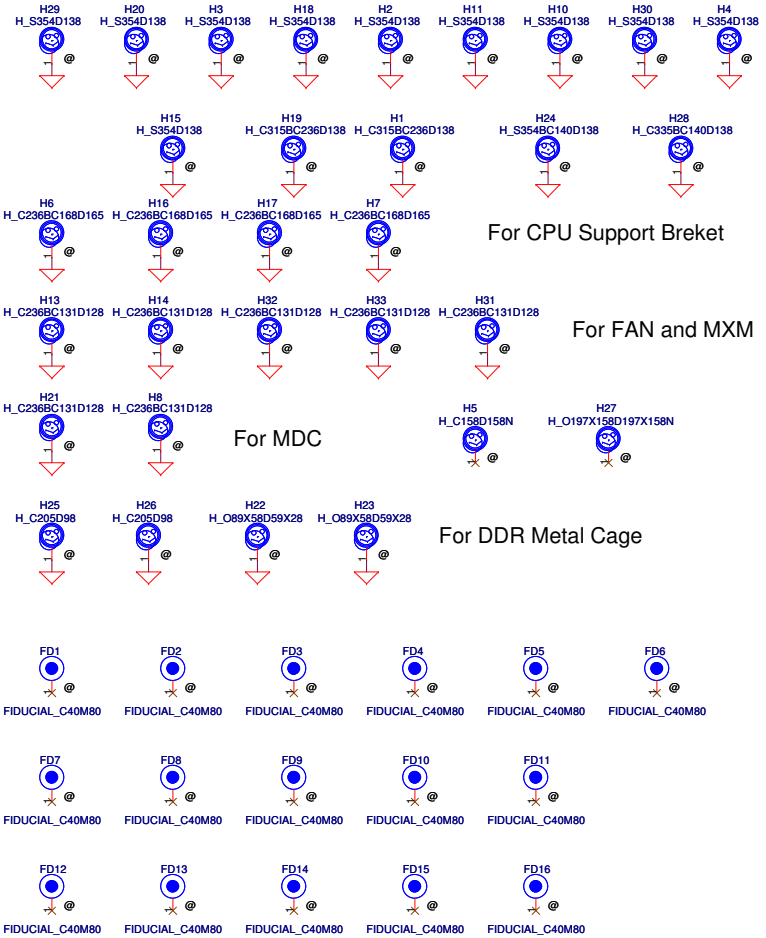
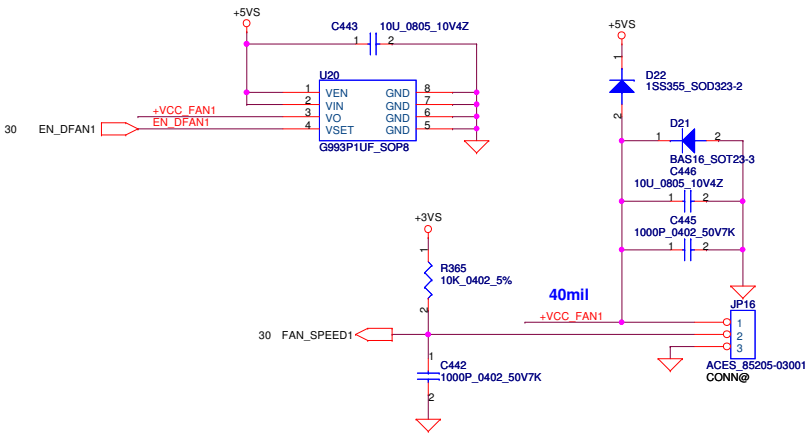


RTC Battery

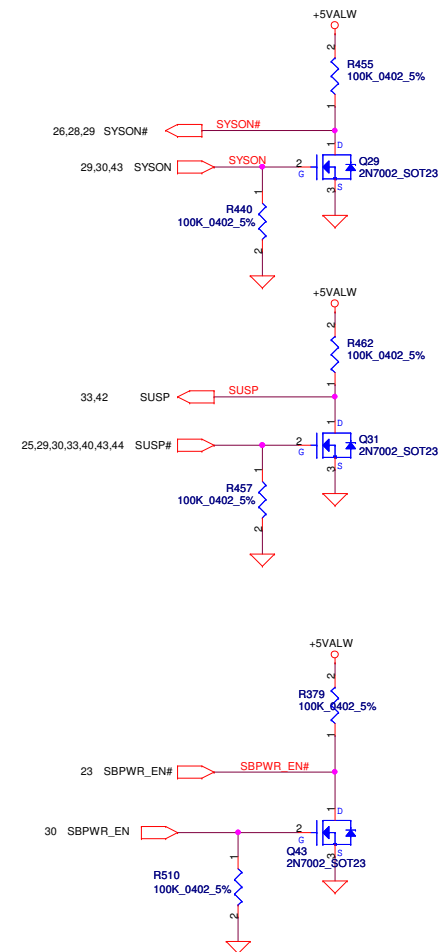
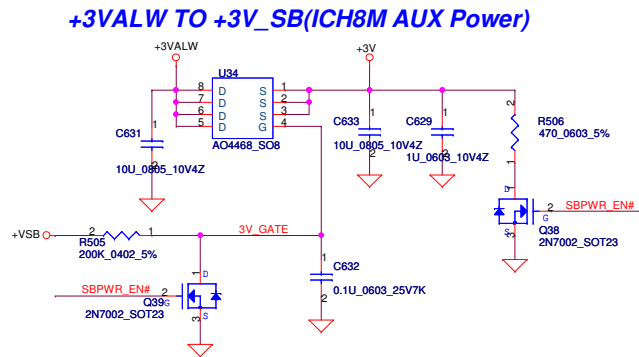
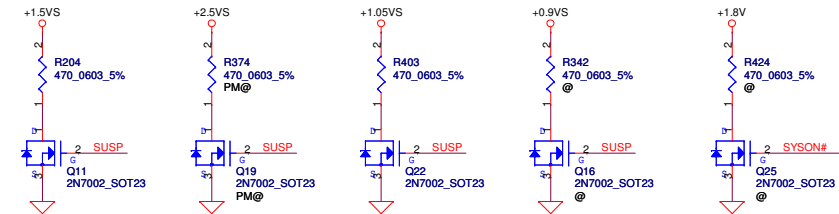
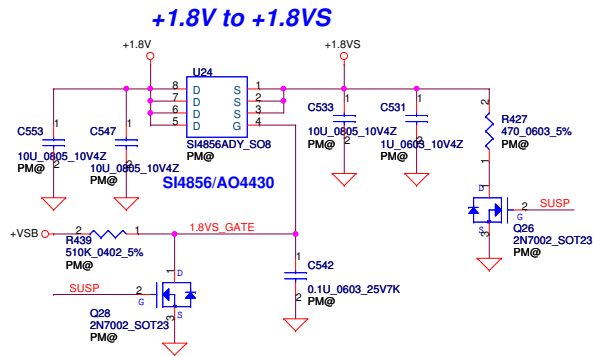
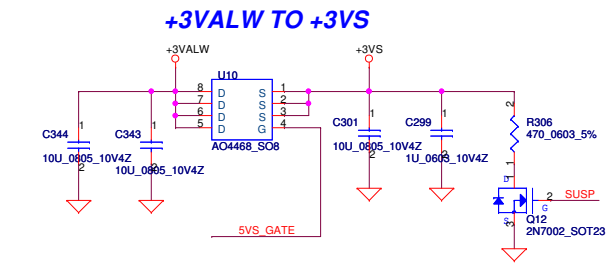
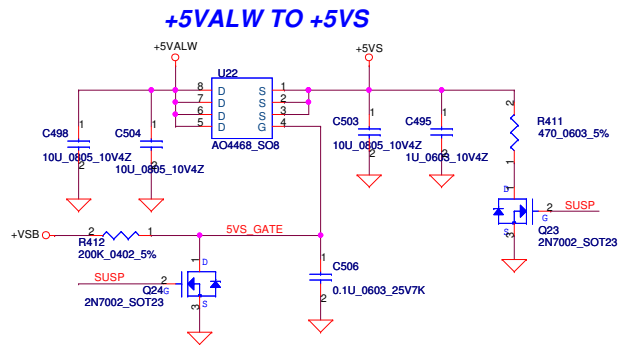


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Size B				Document Number				Rev			
Date: Wednesday, April 18, 2007				ICL50/ICK70 M/B LA-3551P Schematic				33 of 48			

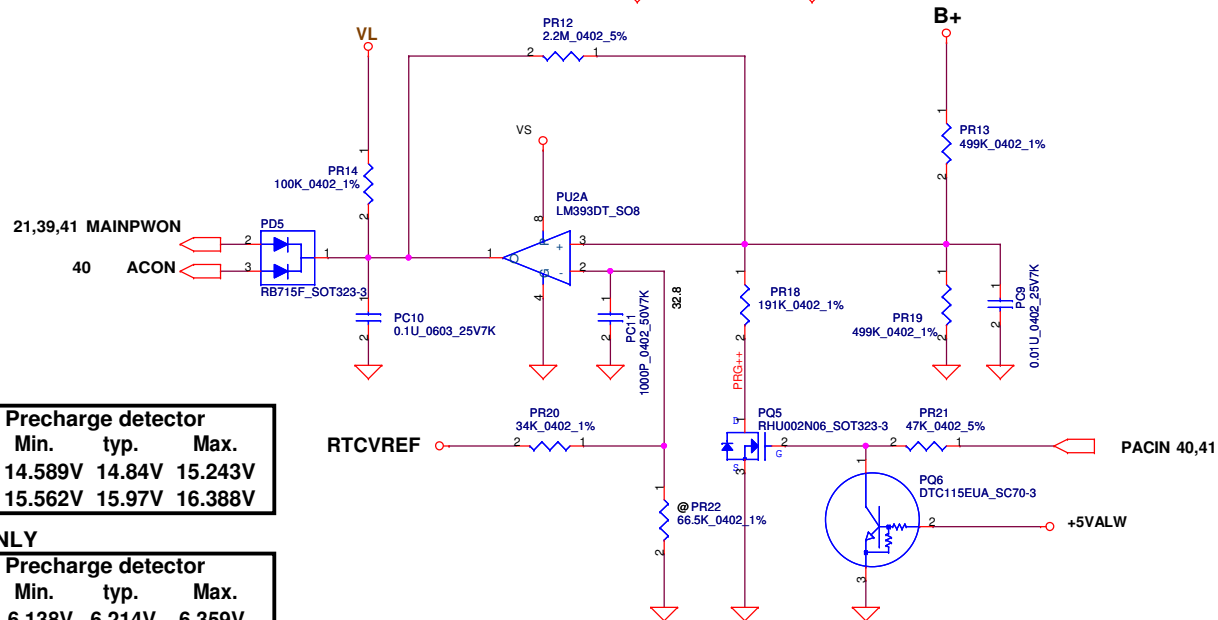
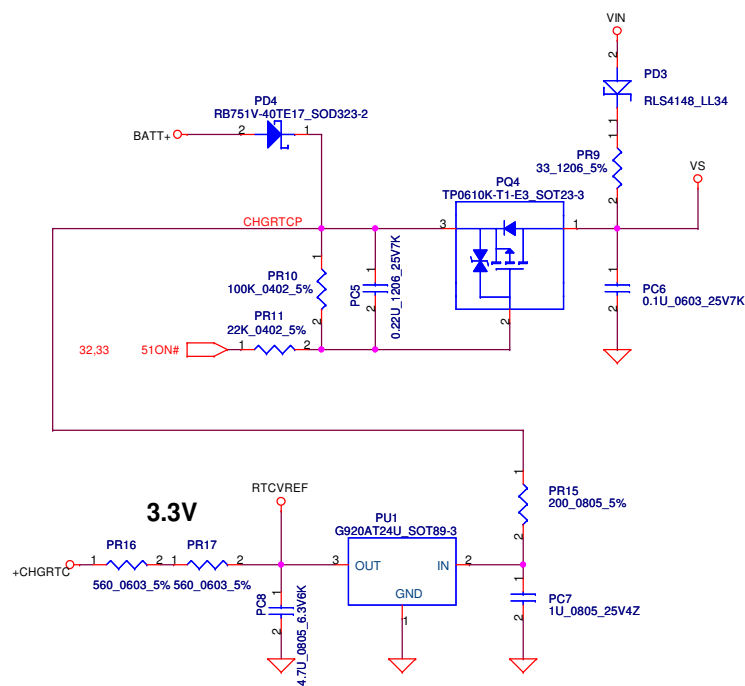
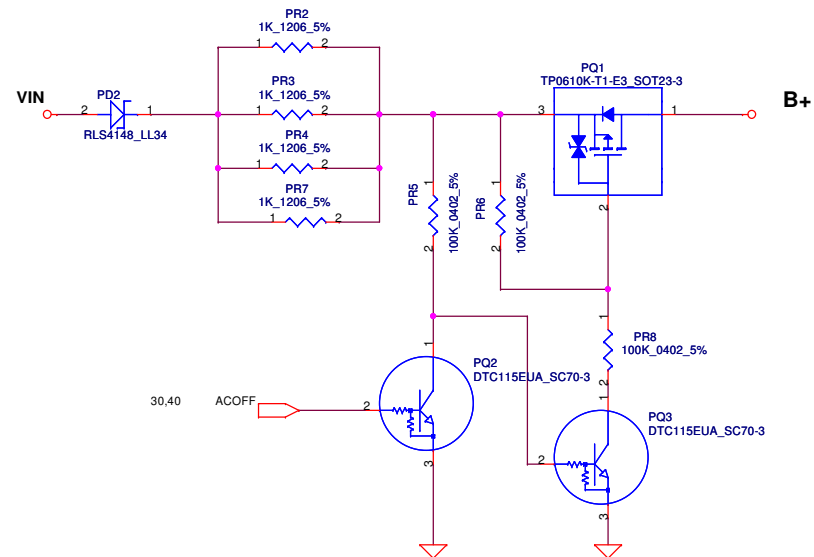
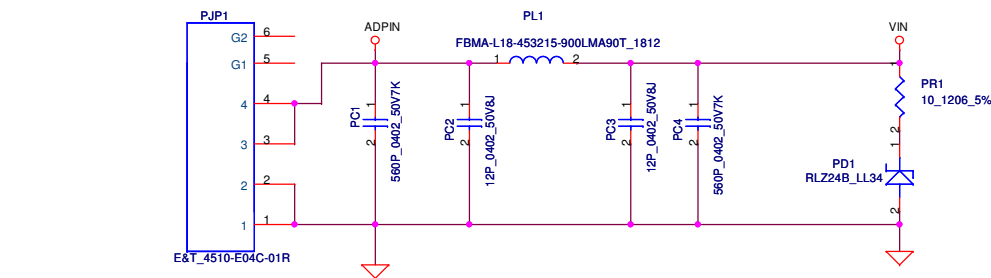
FAN1 Conn



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ACIN

Precharge detector

	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification

Compal Secret Data

Issued Date

2006/08/22

Deciphered Date

2007/08/22

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Compal Electronics, Inc.

Title

DCIN/DECTOR

Size

Document Number

ICL50/ICK70

Rev

1.0

Date:

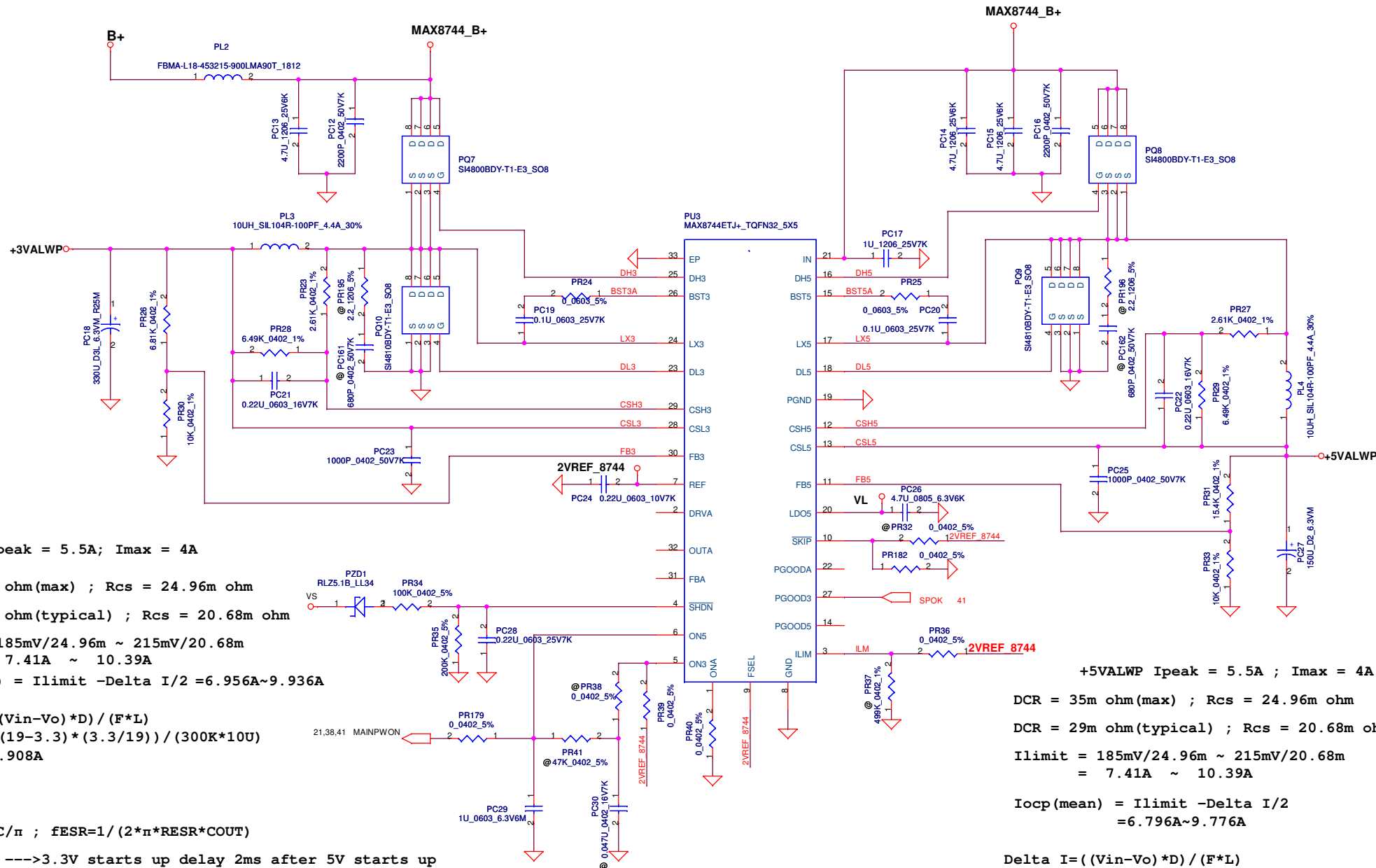
Tuesday, April 10, 2007

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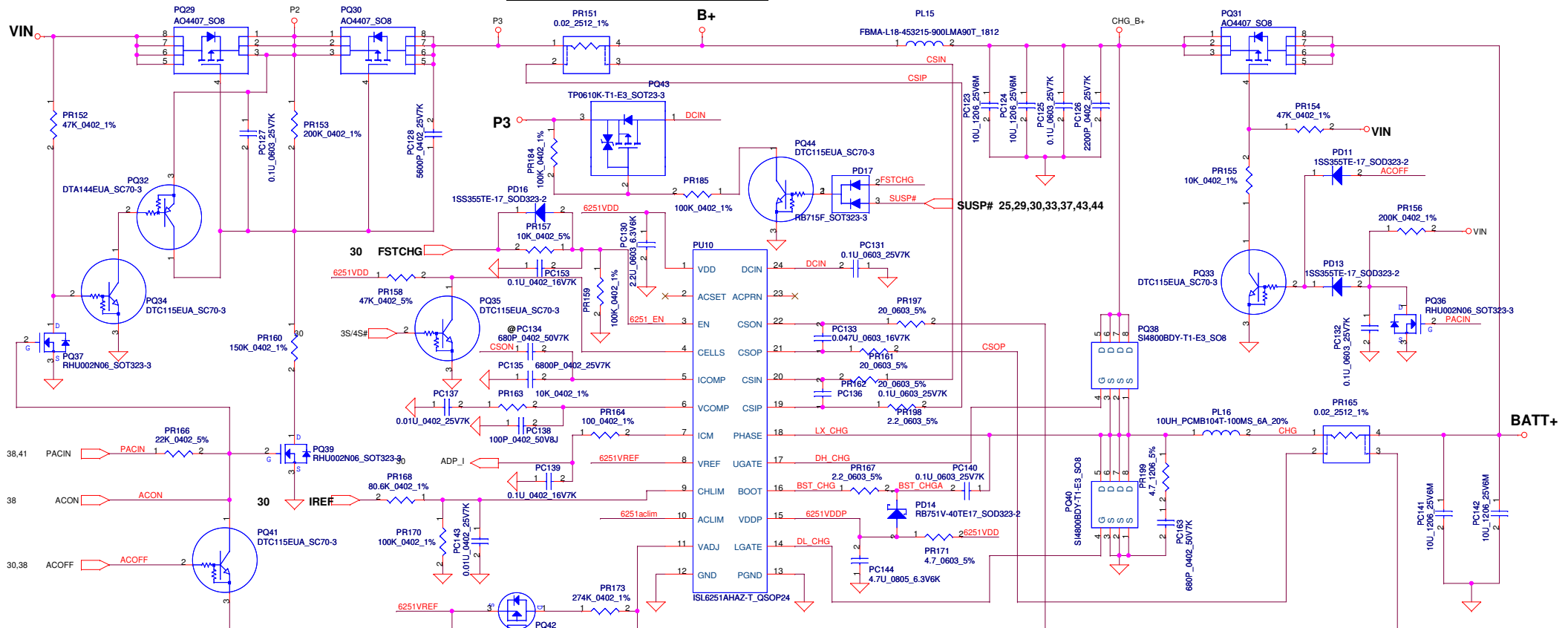


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Iada=0~4.74A (90W)

$$ADP_I = 19.9 \times I_{\text{adapter}} \times R_{\text{sense}}$$

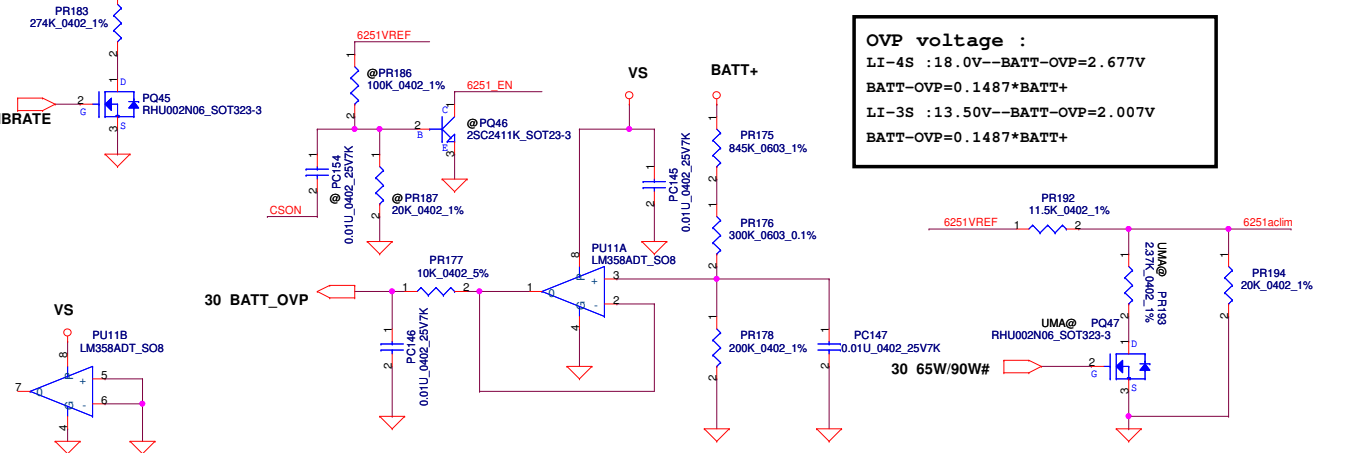
$$CP = 85\% \times I_{\text{ada}} ; CP = 4.07A$$



CP mode
 $I_{\text{input}} = (1/0.02) \times ((0.05 \times V_{\text{acim}}) / 2.39 + 0.05)$
 where $V_{\text{acim}} = 1.502V$, $I_{\text{input}} = 4.07A$
 $V_{\text{acim}} = 2.39 \times ((10K / 152K) / ((5.76K / 152K) + (10K / 152K)))$
 $= 1.502V$

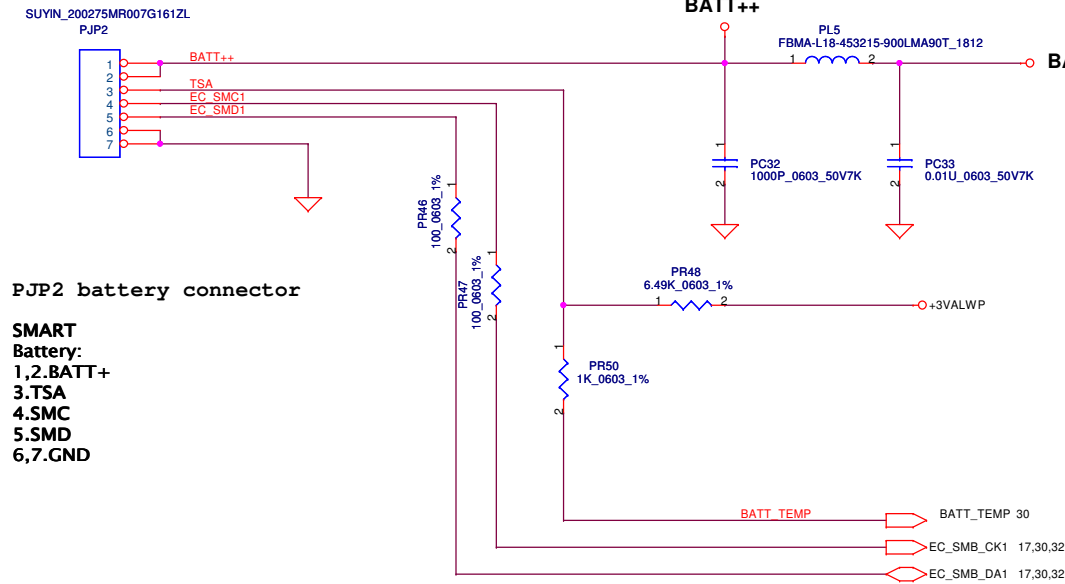
CC=0.6~4.48A
 IREF=0.7224*Icharge
 IREF=0.43V~3.24V

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V



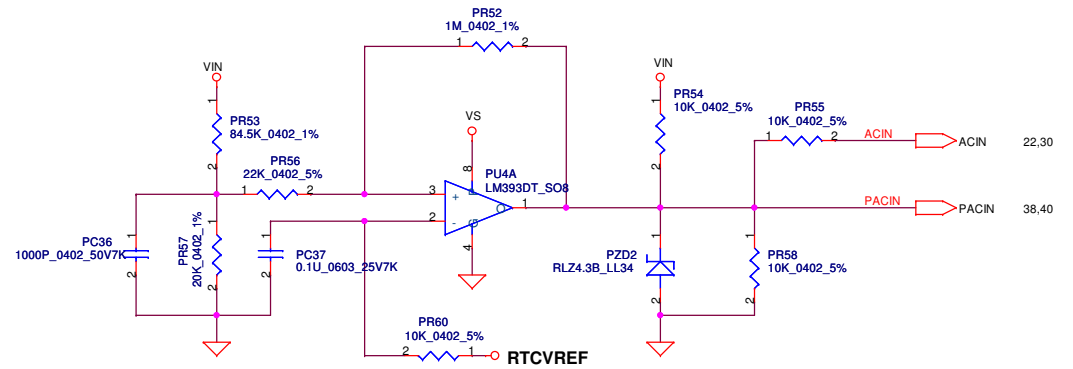
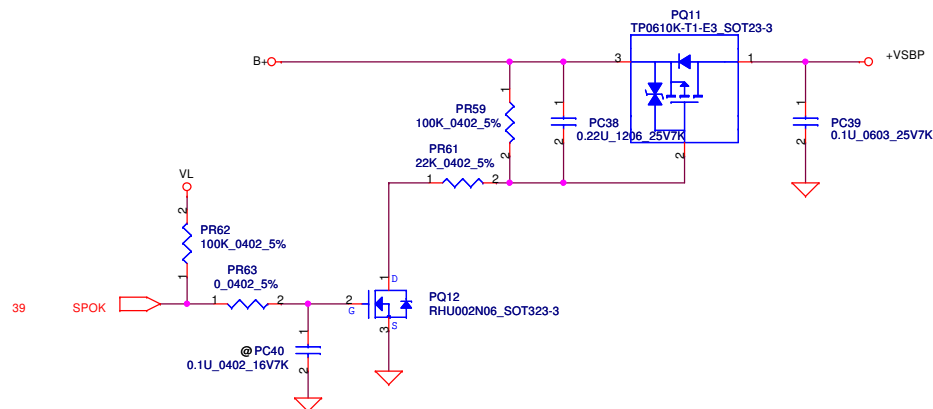
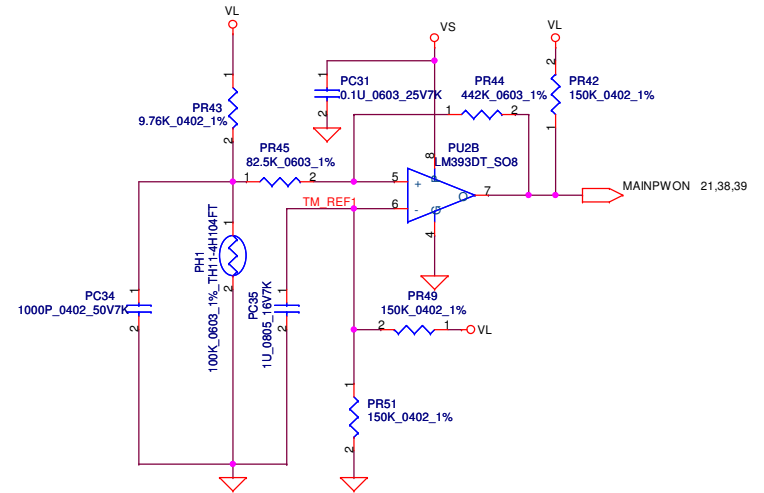
OVP voltage :
 LI-4S : 18.0V--BATT-OVP=2.677V
 BATT-OVP=0.1487*BATT+
 LI-3S : 13.50V--BATT-OVP=2.007V
 BATT-OVP=0.1487*BATT+

PH1 under CPU botten side :
 CPU thermal protection at 90 degree C
 Recovery at 70 degree C



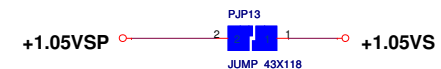
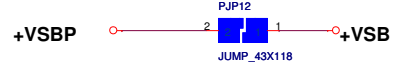
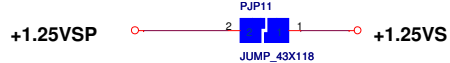
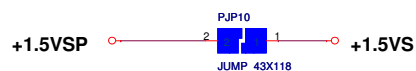
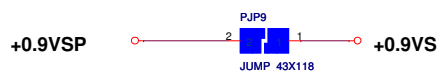
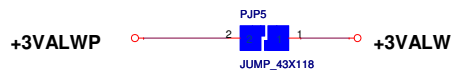
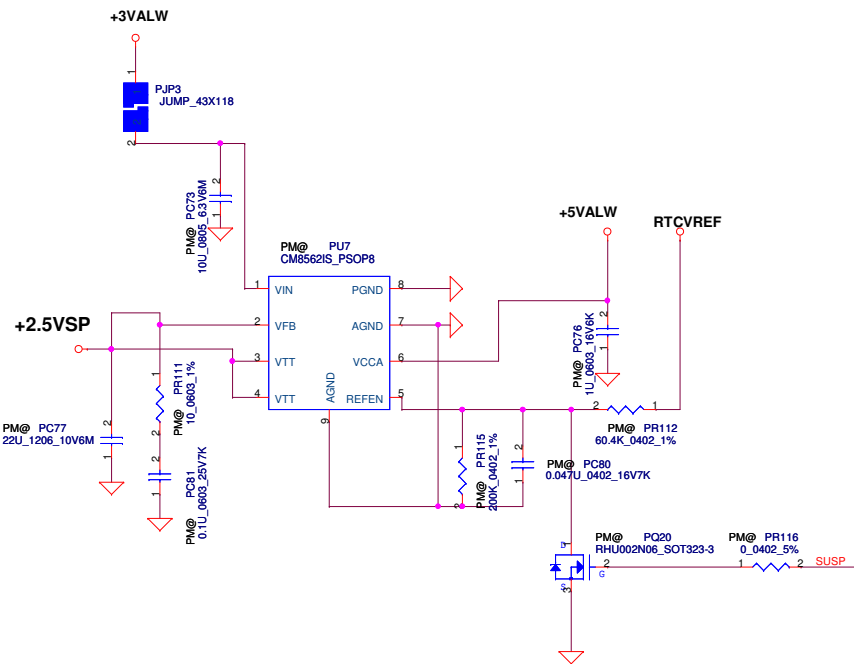
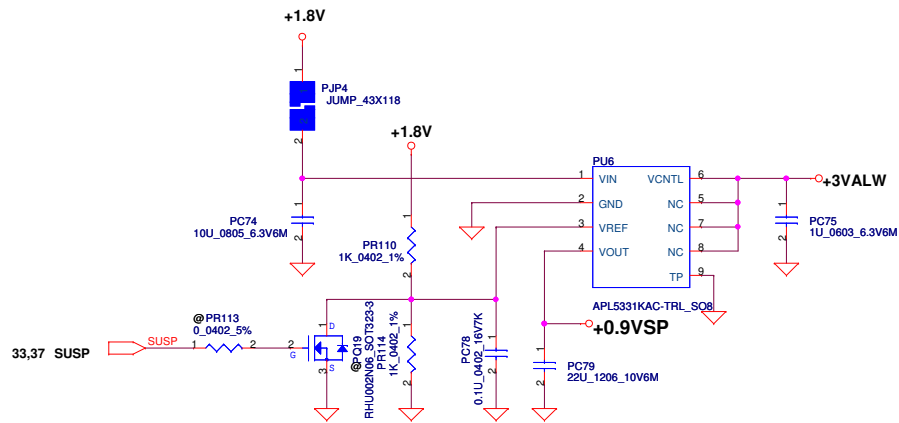
PJP2 battery connector

SMART Battery:
 1,2.BATT+
 3.TSA
 4.SMC
 5.SMD
 6,7.GND

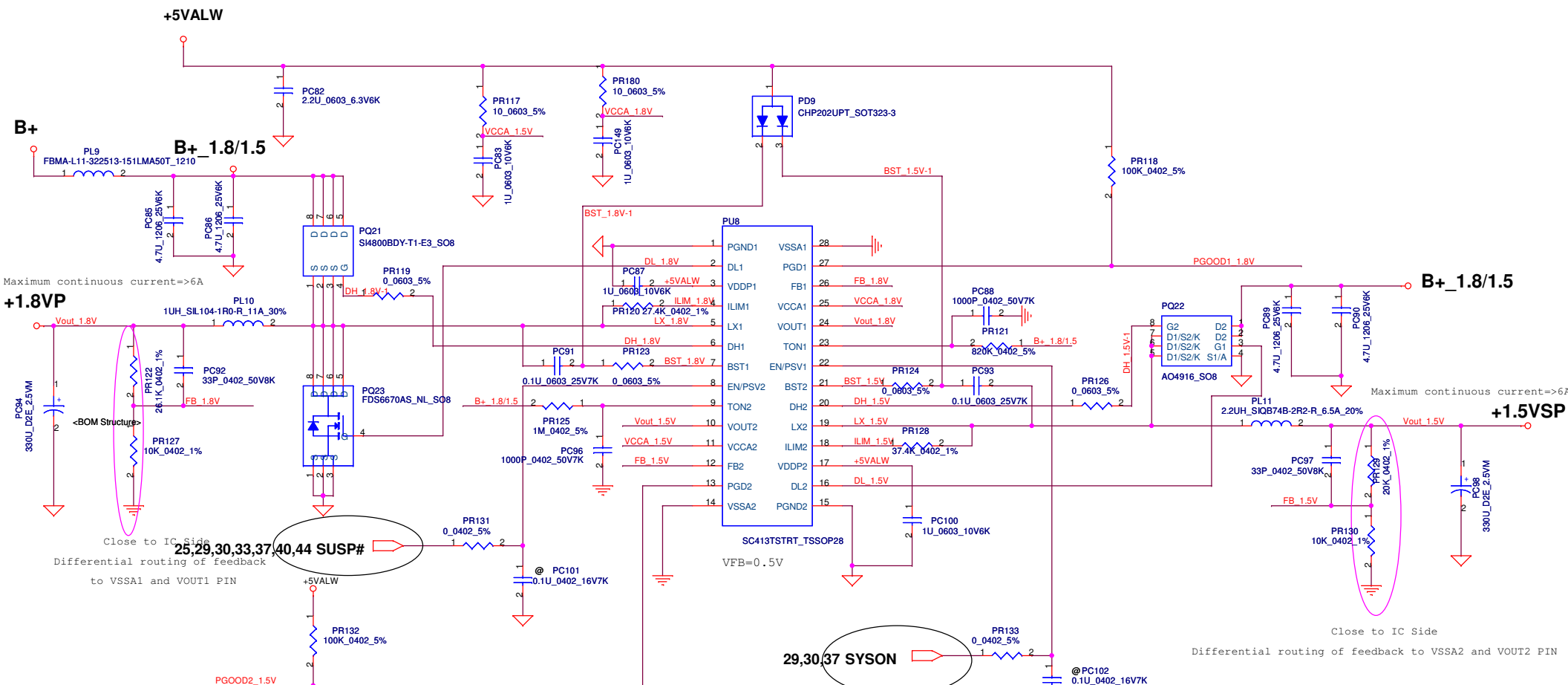


Vin Detector		
Min.	typ.	Max.
H-->L	16.976V	17.257V
L-->H	17.430V	18.384V

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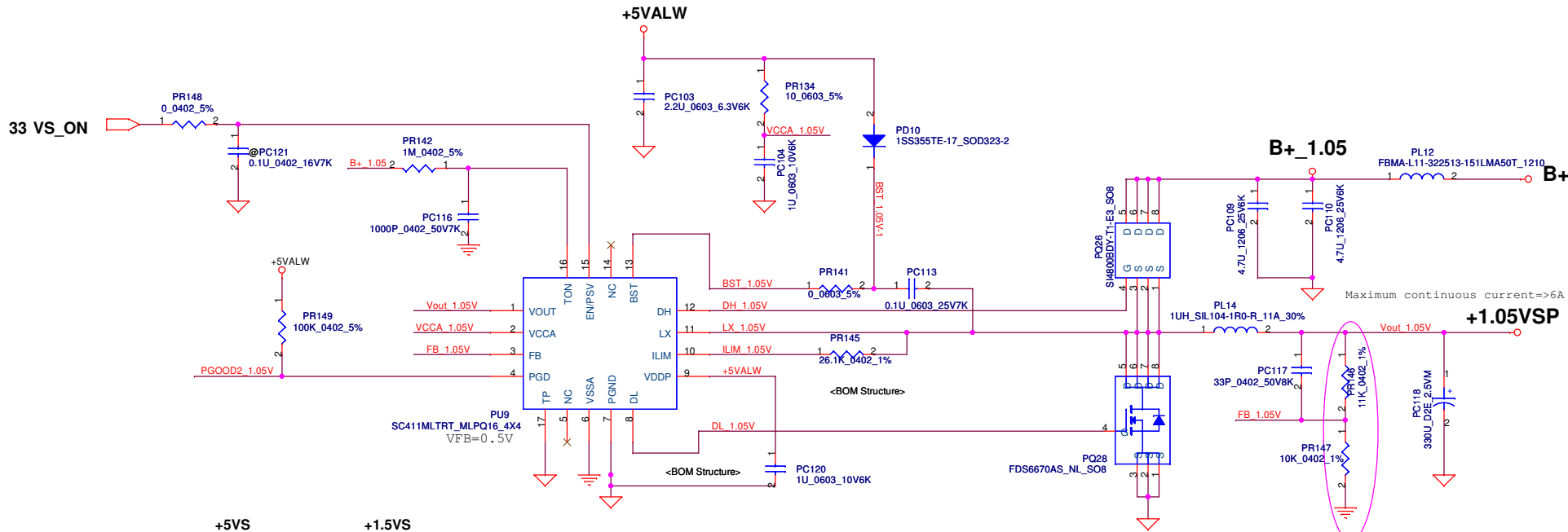
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VFB=0.5V
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$
Ipeak=11.73A, I_{max}=8.211A
 $Ton = (3.3E-12 * (PR121 + 37K) * (Vout / VBat)) + 50ns$
 $= 3.3 * 10e-12 * (820K + 37K) * (1.8 / 19) + 50ns = 0.3179us$
FDS6670AS:Rds(on)=>Typ:9 mOhm
Max:11.5 mOhm
 $I_{ocp} = I_{valley} + I_{ripple} / 2$
 $I_{ripple} = (vin - vout) * (Ton / L) = 5.467A, 1/2 I_{ripple} = 2.734A$
 $I_{valleymin} = 10E-6 * (PR120 / Rds(ON))_{max} * 1.5$
= 9*10e-6 * (27.4K / 0.0115*1.5) = 14.295A > 11.73*1.2 = 14.076A
 $I_{valleymax} = 10E-6 * (PR120 / Rds(ON))_{typ} * 1.2$
 $= 11 * 10e-6 * (27.4K / 0.009 * 1.2) = 27.907A$
OCP==>17.029A~30.641A

VFB=0.5V
 $V_o = VFB * (1 + PR129 / PR130) = 1.5V$
Ipeak=4.39A+2.91A=7.3A, I_{max}=7.3*0.7=5.11A
 $Ton = (3.3E-12 * (PR125 + 37K) * (Vout / VBat)) + 50ns$
 $= 0.3201us$
AO4916 Rds(on)=>Typ:21 mOhm
Max:27 mOhm
Ivalleymin=9*E-6 * (37.4K / 0.027*1.4) = 8.904A > 7.3*1.2 = 8.76A
 $I_{valleymax} = 11 * E-6 * (37.4K / 0.021 * 1.1) = 17.809A$
 $I_{ripple} = (vin - vout) * (Ton / L) = 2.546A, 1/2 I_{ripple} = 1.273A$
 $I_{ocp} = I_{valley} + I_{ripple} / 2$
OCP==>10.177A~19.082A

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Close to IC Side
Differential routing of feedback to VSSA2 and VOUT2 PIN

VFB=0.5V, Ipeak=14.02A, Imax=9.814A

The current rating of +1.05VSP include +VCC_GFX current.

$V_o = VFB * (1 + PR146 / PR147) = 1.05V$

$Ton = (3.3E-12 * (PR142 + 37K) * (Vout / VBat)) + 50ns = 0.2391\mu s$

SI4810BDY: Rds(on) => Typ: 9mOhm
Max: 11.5 mOhm

$Ivalleymin = 9 * 10E-6 * (PR145 / Rds(ON)) * max(1.5)$

= 9 * 10E-6 * (26.1K / (0.0115 * 1.5)) = 13.617A

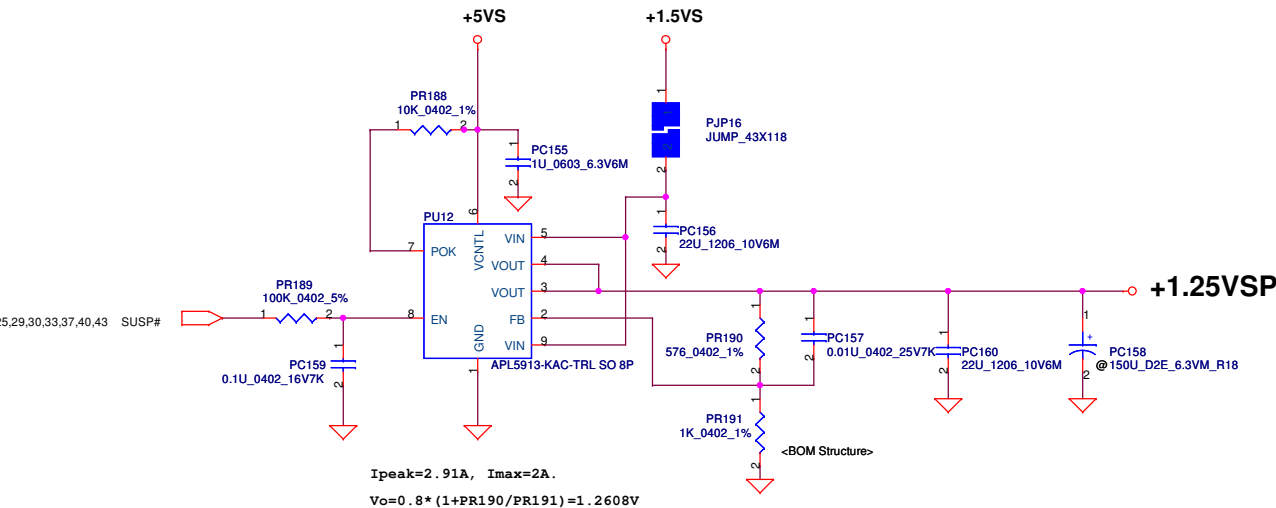
$Ivalleymax = 11 * 10E-6 * (PR145 / Rds(ON)) * min(1.2)$

$= 11 * 10E-6 * (26.1K / (0.009 * 1.3)) = 20.076A$

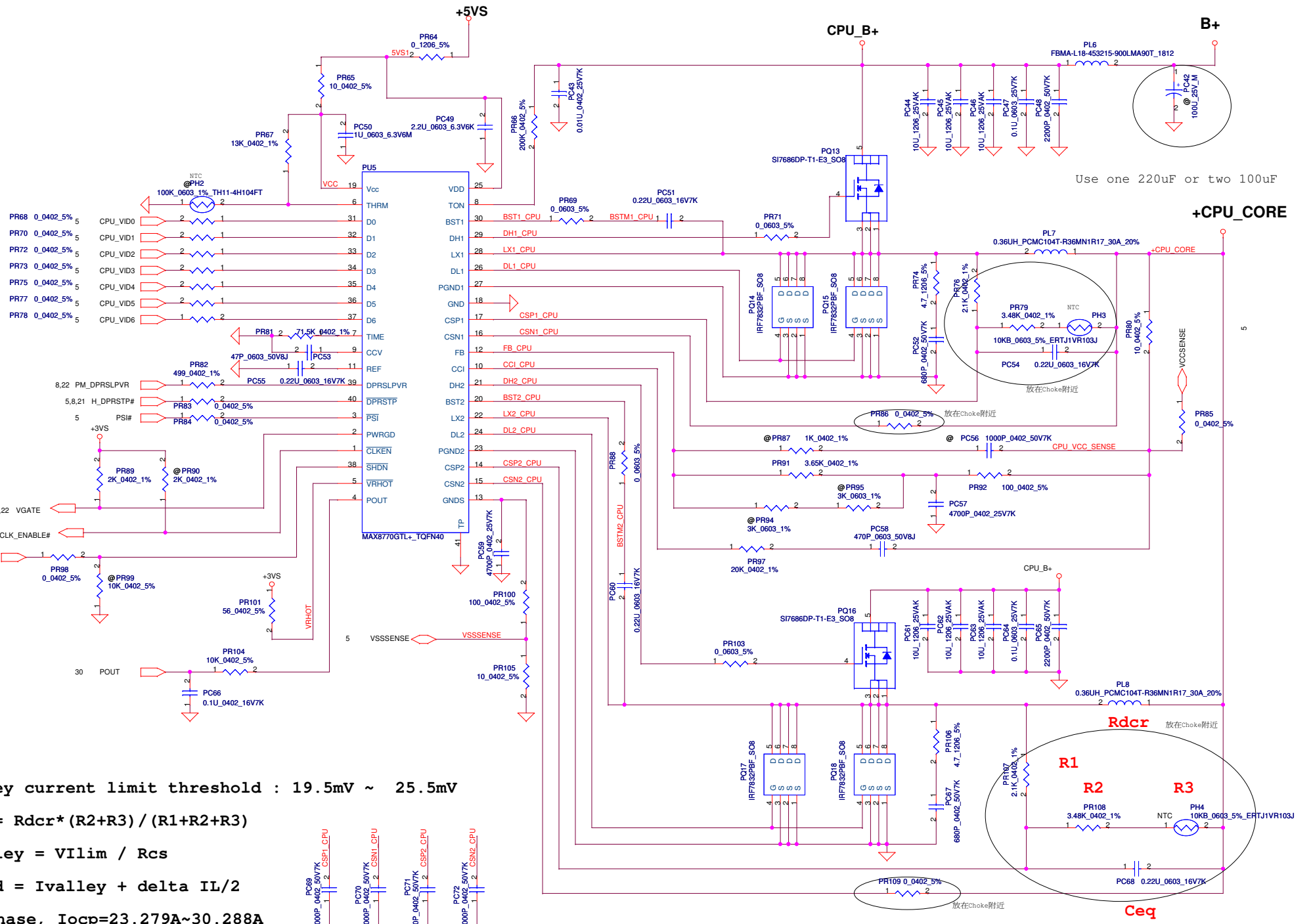
$Iripple = (vin - vout) * (Ton / L) = 4.292A, 1/2 Iripple = 2.146A$

$Iocp = Ivalley + Iripple / 2$

OCP ==> 15.763A ~ 22.222A



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Valley current limit threshold : 19.5mV ~ 25.5mV

$$R_{cs} = R_{dcr} * (R_2 + R_3) / (R_1 + R_2 + R_3)$$

$$I_{valley} = V_{lim} / R_{cs}$$

$$I_{load} = I_{valley} + \Delta I_L / 2$$

Per phase, $I_{ocp} = 23.279A \sim 30.288A$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU_CORE high side MOS desine change	In order to prevent EOL of SI7840, change to SI7686.	0.1	45	Change PQ13 and PQ16 form SB578400080(S TR SI7840DP-T1-E3 1N SO8) to SB000008L80(S TR SI7686DP-T1-E3 1N SO8) .	10/30/06	EVT
2	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ43 SB906100210(S TR TP0610K)	12/21/06	DVT
3	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ44 SB301150000(S TR DTC115EUA)	12/21/06	DVT
4	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD16 SC1SS355010(S DIO 1SS355) Delete PD12 SC1SS355010(S DIO 1SS355)	12/21/06	DVT
5	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD17 SCSB715F000(S DIO RB715F)	12/21/06	DVT
6	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR184,PR185 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
7	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC153 SE076104K80(S CER CAP 0.1U 0402 16V K X7R)	12/21/06	DVT
8	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ45 SB502060000(S TR RHU002N06)	12/21/06	DVT
9	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ46 SB324110010(S TR 2SC411K)	12/21/06	DVT
10	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR183 SD034274380(S RES 1/16W 274K 0402 1%)	12/21/06	DVT
11	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR186 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
12	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR187 SD034200280(S RES 1/16W 20K 0402 1%)	12/21/06	DVT
13	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC154 and PC146 SE075103K80(S CER CAP 0.01U K 25V X7R 0402)	12/21/06	DVT
14	Noise issue in S3 mode and idle mode.	In order to prevent noise issue in S3 mode and idle mode.	0.2	40	Add PC42 SF22004M210(S CAP 220U_25V_M)	12/21/06	DVT
15	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Change PR157 from SD028000080(s res 1/16w 0 0402 5%) TO SD0281000280(S RES 1/16W 10K 0402 5%)	12/21/06	DVT
16	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR34 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100380(S RES 1/16W 100K 0402 5%)	12/21/06	DVT
17	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR35 SD028100380(S RES 1/16W 100K 0402 5%) to SD028200380(S RES 1/16W 200K 0402 5%)	12/21/06	DVT
18	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PC28 from SE042104K80(S CER CAP 0.1U 25V K X7R 0603) to SE000005ZM8(S CER CAP 0.22U 25V K X7R 0603)	12/21/06	DVT
19	CPU MOSFET switching has interference.	Improve CPU switching interference.	0.2	45	Change PC69,PC70,PC71,PC72 from SE082221J80 to SE068102J80 (S CER CAP 1000P 25V J NPO 0402)	12/21/06	DVT
20	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PU7 SA085620080 from X63470BOL01.	12/21/06	DVT
21	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PQ20 SB502060000 from X63470BOL01.	12/21/06	DVT
22	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR111 SD014100A80 from X63470BOL01.	12/21/06	DVT
23	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR112 SD034604280 from X63470BOL01.	12/21/06	DVT

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1	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR115 SD034200380 from X63470BOL01.	10/30/06	EVT
2	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR116 SD028000080 from X63470BOL01.	12/21/06	DVT
3	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC73 SE142475K80 from X63470BOL01.	12/21/06	DVT
4	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC76 SE135105K80 from X63470BOL01.	12/21/06	DVT
5	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC77 SE116226M80 from X63470BOL01.	12/21/06	DVT
6	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC80 SE076473K80 from X63470BOL01.	12/21/06	DVT
7	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC81 SE042104K80 from X63470BOL01.	12/21/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ25 SB548000310(S TR SI4800BDY).	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ27 SB548100020(S TR 4810BDY)	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PD10 from SC1P202U010 to SC1SS355010.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR135 SD034100380.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR140,SD013000080, PR150 SD028000080.	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR181 SD013100A80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR139 SD034150280.	12/27/06	DVT
15	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR144 SD034100280	12/27/06	DVT
16	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR137 SD034105280.	12/27/06	DVT
17	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR138 SD028100480.	12/27/06	DVT
18	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC105,PC106 SE142475K80.	12/27/06	DVT
19	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC107,PC151 SE080105K80.	12/27/06	DVT
20	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC108 SE074102K80.	12/27/06	DVT
21	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC111 SE042104K80.	12/27/06	DVT
22	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC112 SE068330K80	12/27/06	DVT
24	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PL13 SH000008Y80.	12/27/06	DVT

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1	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC114 SGA20221D30	12/27/06	DVT
2	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PU9 from SA00001FD80 to SA00001FB80	12/27/06	DVT
3	For SMT BOM convenient.	For SMT BOM convenient.	0.3	40	Change PD14 from SC1H751H010 to SC1B751V010.	12/27/06	DVT
4	Increase _1.5VSP OCP point	Increase _1.5VSP OCP point for +1.25VSP new solution.'	0.3	43	Change PR128 from SD034154280 to SD034374380.	12/27/06	DVT
5	Decrease +1.05VSP OCP point.	Decrease +1.05VSP OCP point.	0.3	44	Change PR145 from SD034324280 to SD034261280		DVT
6	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PU12 SA000015410.	12/27/06	DVT
7	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR188 SD034100280.	12/27/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR189 SD034100380.	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR191 SD034100180.	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR190 SD034576080.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC155 SE107105M80.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC156, PC160 SE116226M80	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC157 SE075103K80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC159 SE076104K80.	12/27/06	DVT
15	Increase +1.5VSP output capacitor.	Increase +1.5VSP output capacitor.	0.3	43	Change PC98 from SGA20221D30 to SGA19331D00	12/27/06	DVT
16	Cost issue.	Cost issue.	0.3	44	Change PC118 from SGA20471D00 to SGA19331D00.	12/30/06	DVT
17	BOM issue.	BOM issue.	0.3	45	Change PH3, PH4 from SL210021F20 to SL200000200	12/30/06	DVT
18	Assembly issue.	Due to assembly hard, delete PC42.	0.3	45	Delete PC42 SM22004M210.	12/30/06	DVT
19	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE142475K80 to SE093106M80	01/04/06	DVT
20	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE153106K80 to SE093106M80	01/04/06	DVT
21	Add pull high resister for VAGTE.	Add pull high resister for VAGTE.	0.4	45	Add PR89 SD034200180 (S RES 1/16W 2K 0402 1%)	01/04/06	DVT
22	Delete PQ46	PQ46 has potential risk to cause system battery OVP.	0.4	40	Delete PQ46 SB324110010 (S TR 2SC411K)	01/04/06	DVT
23	Material shipping issue.	Material shipping issue.	0.4	45	Change PC69, PC70, PC71, PC72 from SE068102J80 to SE074102K80	01/04/06	DVT

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1	Cost down	Cost down	0.5	40	Change PQ38 from SB548100020 to SB548000310.	03/09/07	PVT
2	Cost down	Cost down	0.5	40	Change PQ40 from SB548100020 to SB548000310.	03/09/07	PVT
3	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PR199 SD001470B80(S RES 1/4W 4.7 1206 +-5%)	04/01/07	Pre-MP
4	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PC163 SE074681K80(S CER CAP 680P 50V K X7R)	04/01/07	Pre-MP
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